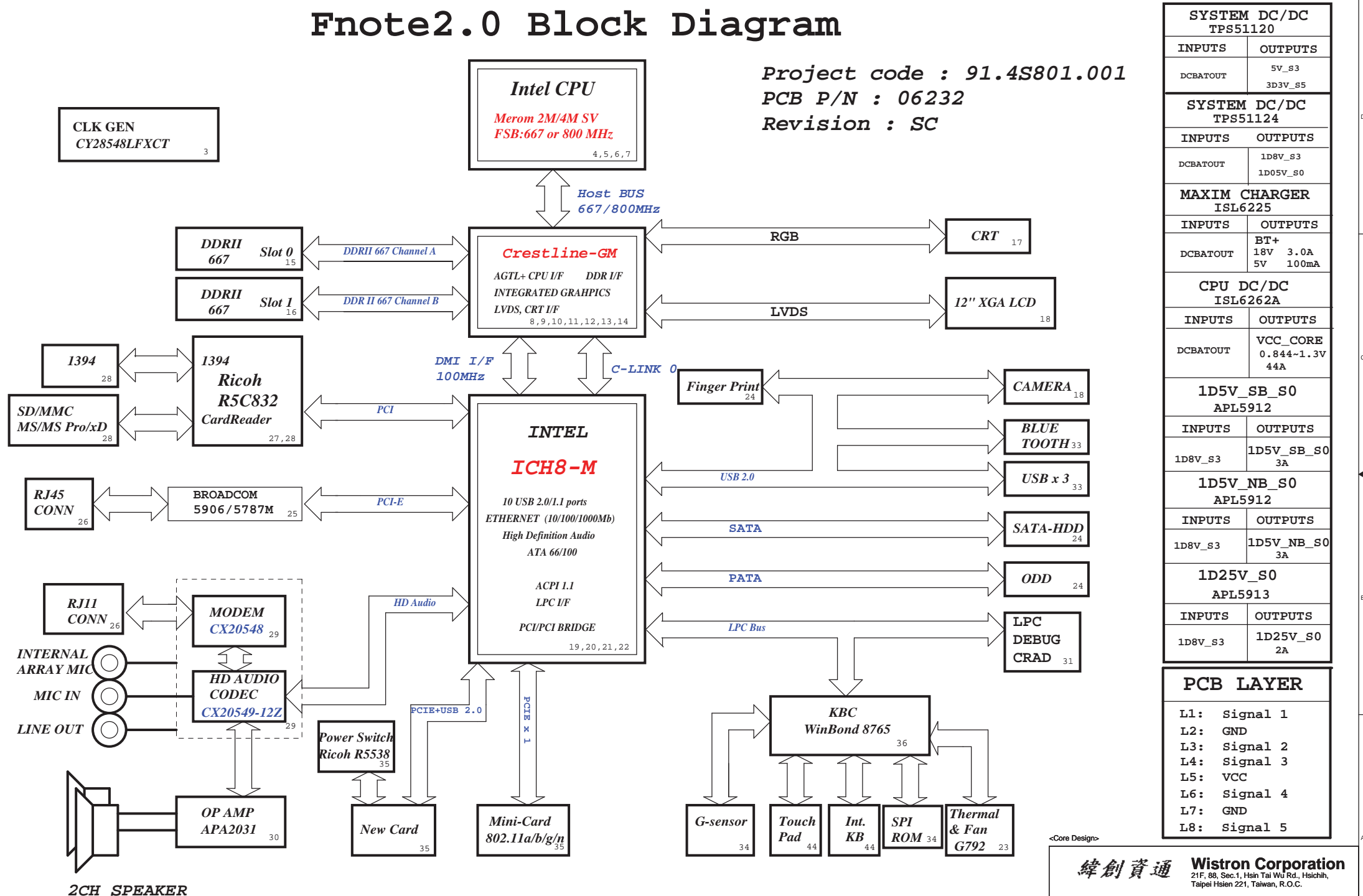


# Fnote2.0 Block Diagram

Project code : 91.4S801.001  
PCB P/N : 06232  
Revision : SC



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title		
Block Diagram		
Size	Document Number	Rev
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Date:	Friday, March 09, 2007	Sheet 1 of 45

## INTEL ICH8-M STRAP PIN

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIe Port Config 1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low at rising edge of PWROK. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC(Config Registers:offset 224h)
HDA_SYNC	PCIe Port Config 1 bit0, Rising Edge of PWROK.	Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#	PCIe Port Config 2 bit0, Rising Edge of PWROK.	Sets bit2 of RPC.PC(Config Registers:Offset 224h)
GPIO20	Reserved	Weak Internal PULL-DOWN.NOTE:This signal should not be pull HIGH.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0# SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
INTVRMEN	Integrated VccSus1_05 VccSUS1_5 and VccCL1_5 VRM Enable/Disable.Always sampled.	Enables integrated VccSus1_05,VccSUS1_5 and VccCL1_5 VRM when sampled high
LAN100_SLP	Integrated VccLAN1_05 VccCL1_05 VRM enable /Disable. Always sampled.	Enables integrated VccLAN1_05,VccCL1_05 VRM when sampled high
SATALED#	PCIe LAN REVERSAL.Rising Edge of PWROK.	This signal has weak internal pull-up. set bit27 of MPC.LR(Device28:Function0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH8M will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.(Offset:3410h:bit5)
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK.	Internal Pull-Up.If sampled low,the Flash Descriptor Security will be overridden.if high,the Security measures defined in the Flash Descriptor will be in effect. This should only be used in manufacturing environments

XOR Chain Entrance Strap		
ICH_RSVP3	AZ_DOUT_ICH	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation(default)
1	1	Set PCIe port config bit1

A16 swap override strap	
PCI_GNT#3	low = A16 swap override enable high = default

BOOT BIOS Strap		
PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPT
1	0	PCT
1	1	LPC(Default)

Integrated VccSus1_05,VccSus1_5,VccCL1_5		
SM_INTVRMEN	High=Enable	Low=Disable
Integrated VccLan1_05VccCL1_05		
LAN100_SLP	High=Enable	Low=Disable

DEFAULE HIGH

No Reboot Strap	
SPKR	LOW = Defaule
	High=No Reboot

8.2K PULL HIGH

## INTEL CRESTLINE STRAP PIN

## PCI Routing

CFG Strap	LOW 0	HIGH 1
CFG 5	DMI X 2	DMI X 4 ★
CFG 8 Low Power PCI Express	Normal★	Low Power mode
CFG 9 PCI Express Graphics Lane Reversal	Lane Reversal	Normal Mode(Lanes number in order)★
CFG 16 FSB Dynamic ODT	Disabled	Enabled★
CFG 19 DMI Lane Reserved	Normal Operation★	Reserved Lane
CFG 20 Concurrent SDVO/PCIe	Only PCIe or SDVO is operation★	PCIe and SDVO are operation simultaneous
SDVO_CTRL_DATA	NO SDVO Card Present★	SDVO Card Present

CFG 12	XOR/ALL-Z
CFG 13	Reserved
LL(00)	Reserved
LH(01)	XOR Mode Enabled
HL(10)	All Z Mode Enabled
HH(11)	Normal Operation

	IDSEL	IRQ	REQ/GNT
R5C832	25	A/C	0

## History

09/13 drawing SA

11/03 drawing SB

01/11 drawing SC

## INTEL ICH8-M INTEGRATED PULL-UPS and PULL-DOWNS

SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K,but it is only enabled when in s3.
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
LDA[3:0]#/FWH[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 20K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH_[3:0]	PULL-UP 20K
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CL_RST#	PULL-UP 13K

Update:

MCH: 71.CREST.M02

ICH : 71.0ICH8.00U

LAN:71.05906.B03

CHARGER:74.06255.A73

KBC:71.08765.A0G

SB

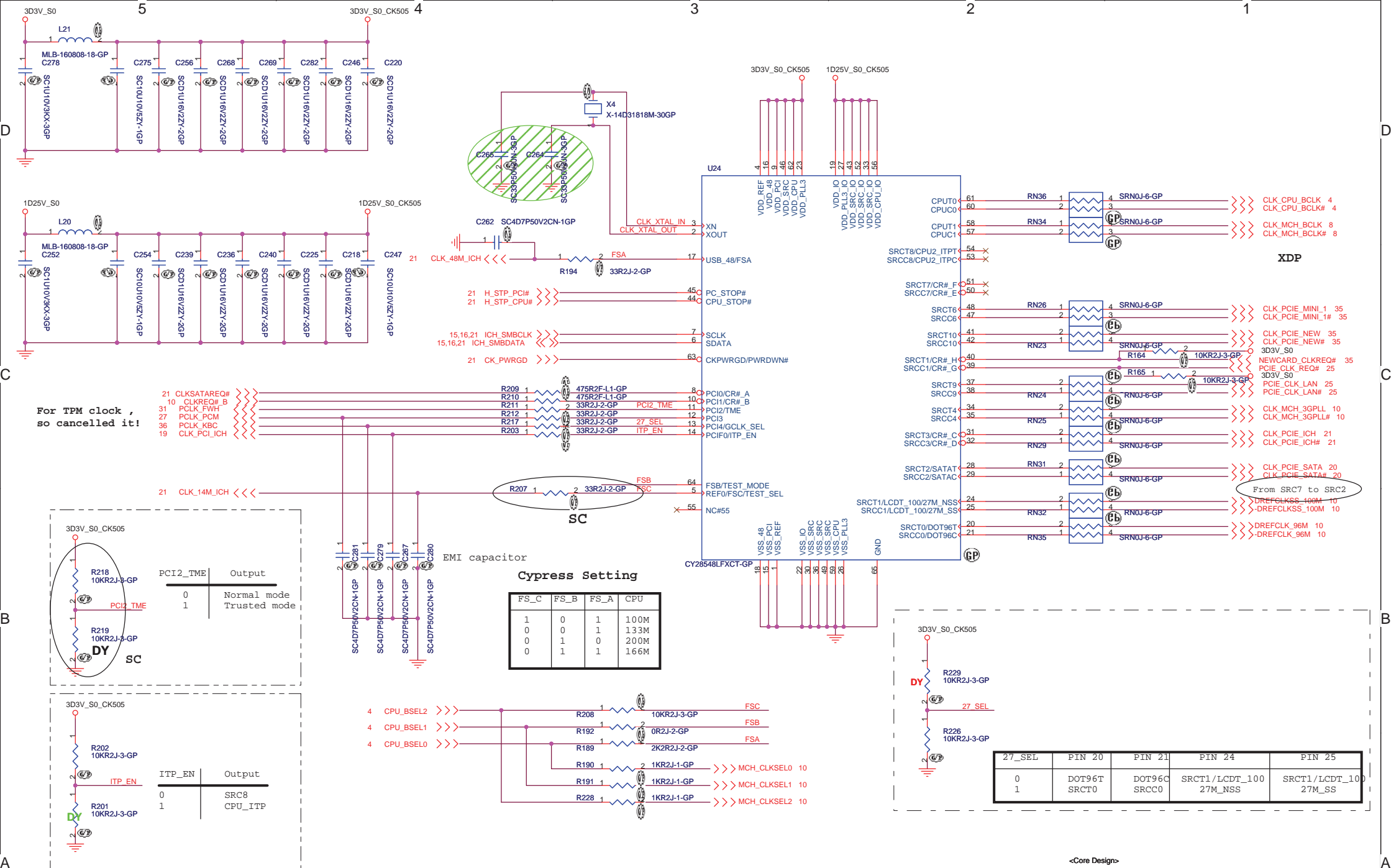
06/11/06



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Title	Document Number	F-note 2.0	Rev SC
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Design Note:

- All of Input pin didn't have internal pull up resistor.
- Clock Request (CR) function are enable by registers.
- CY28548 integrated serial resistor of differential clock, as shown in the schematic.

WWW.AliSaler.Com

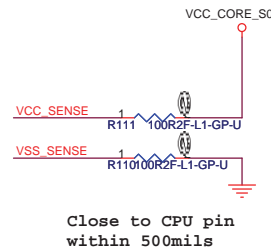
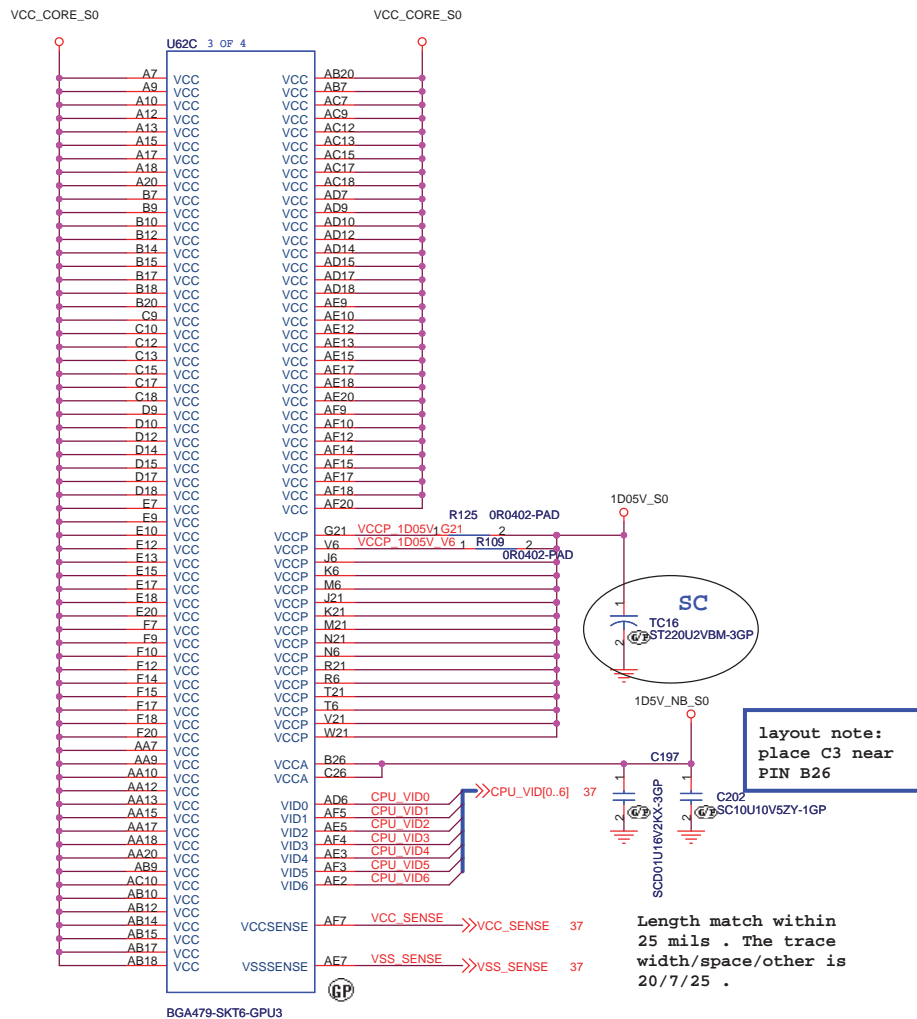
0 = CR#\_A-SRC0, 1 = CR#\_A-SRC2  
 0 = CR#\_B-SRC1, 1 = CR#\_B-SRC4  
 0 = CR#\_C-SRC0, 1 = CR#\_C-SRC2  
 0 = CR#\_D-SRC1, 1 = CR#\_D-SRC4  
 CR#\_G controls SRC9, CR#\_H controls SRC10  
 CR#\_E controls SRC6, CR#\_F controls SRC8

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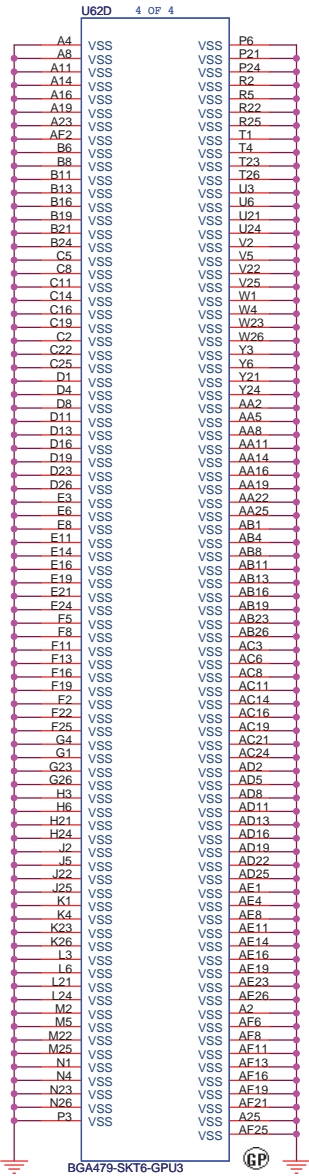
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 Size A3 Document Number: **F-note 2.0** Rev **SC**  
 Date: Friday, March 09, 2007 Sheet 3 of 45



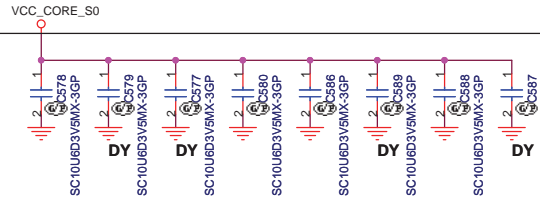


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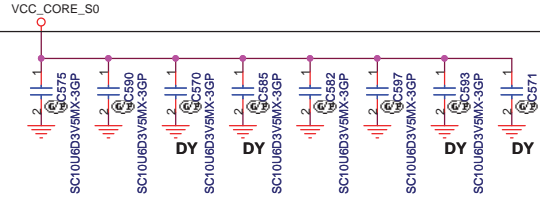
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Size	
A3	
Document Number	
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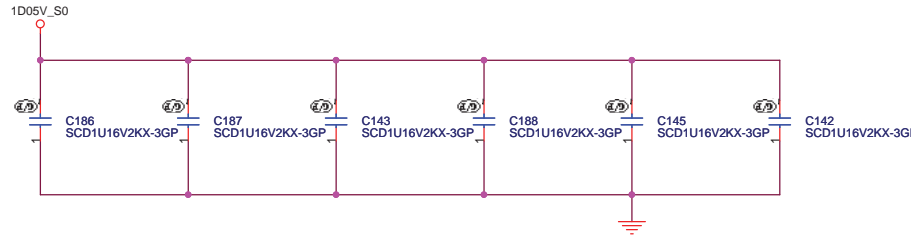
Place these capacitors on L1  
(North side ,Secondary Layer)



Place these capacitors on L1  
(North side ,Secondary Layer)



Mid Freqenced  
Decoupling



Place these  
inside socket  
cavity on L1  
(North side  
Secondary)

<Core Design>

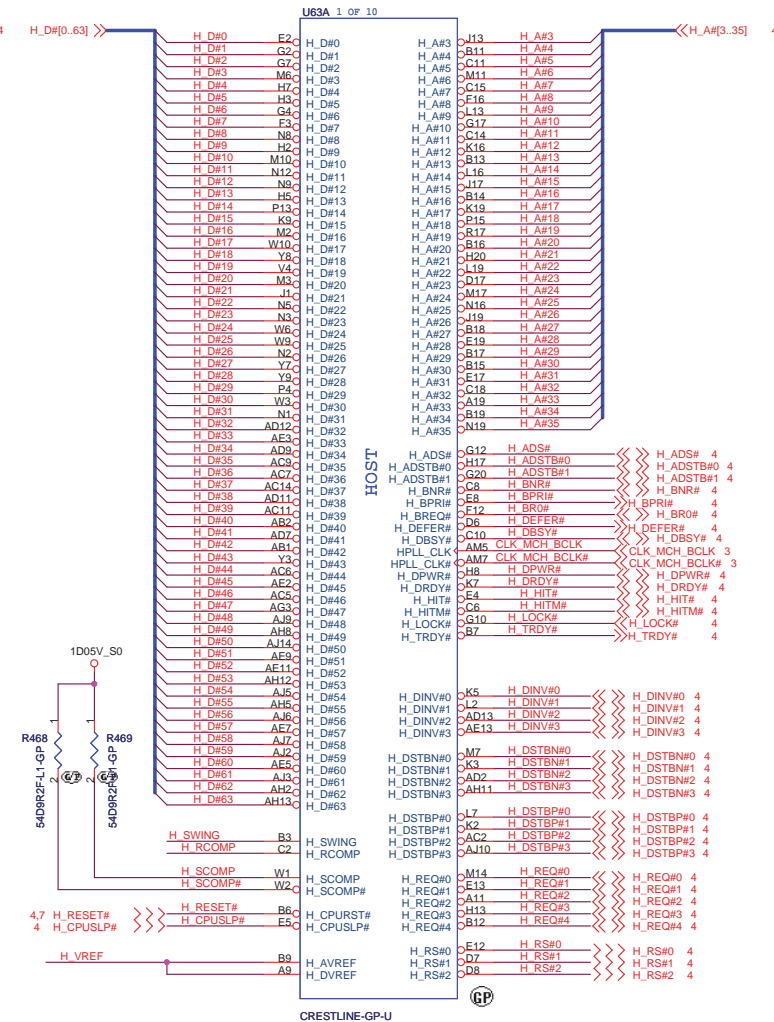
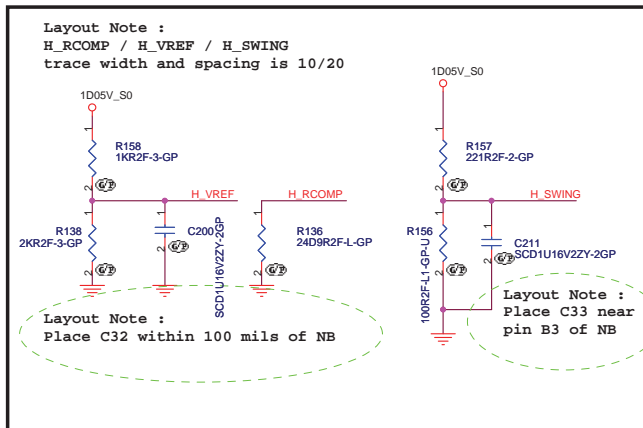
緯創資通 Wistron Corporation  
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Title		
Meron(3/3)-GND&Bypass		
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layout note :  
Route H\_SCOMP and H\_SCOMP# with trace width, spacing  
and impedance (55 ohm) same as FSB data traces

Layout Note :  
H\_RCOMP / H\_VREF / H\_SWING  
trace width and spacing is 10/20

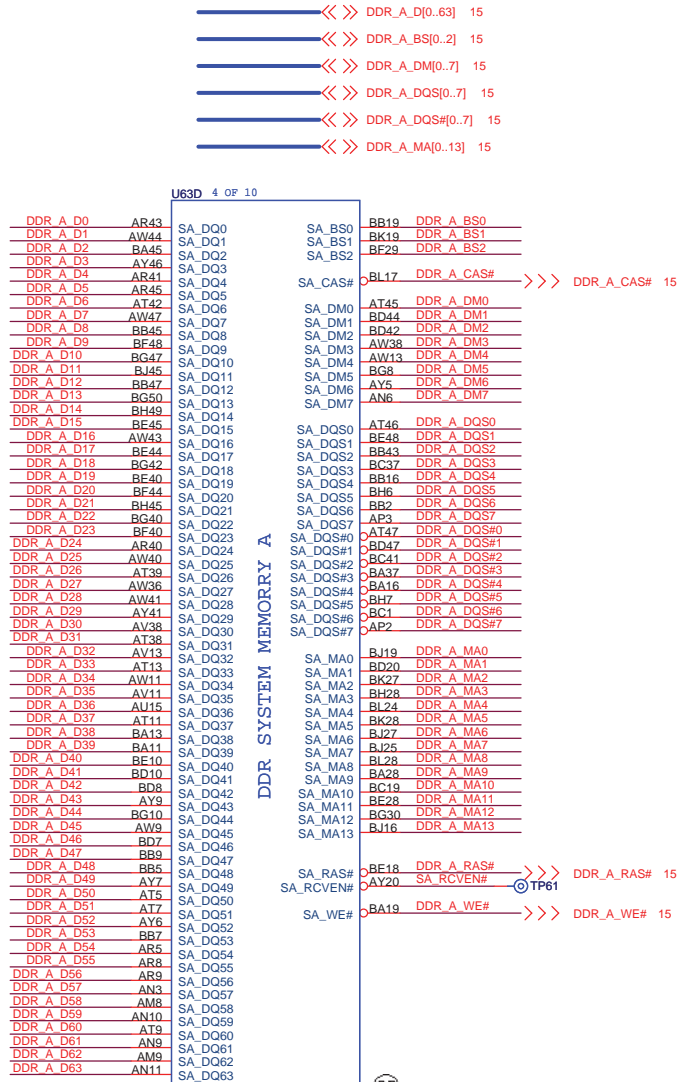


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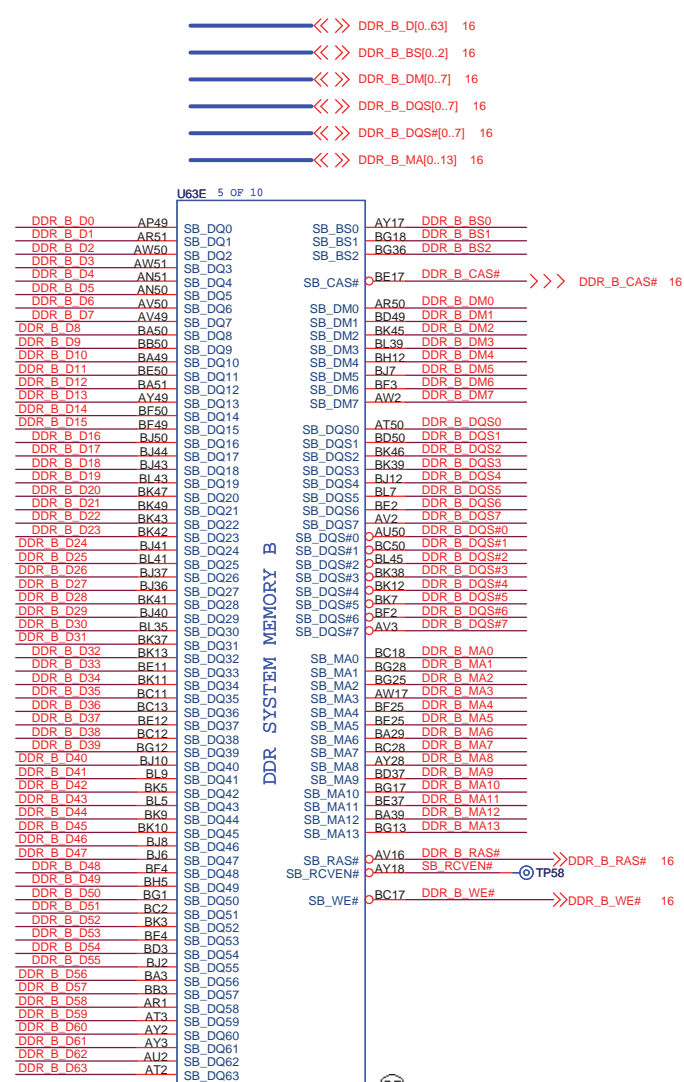
緯創資通

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Title		CRESTLINE(1/6)-AGTL+/DMI/DDR2	
Size	Document Number	Sheet	8 of 45
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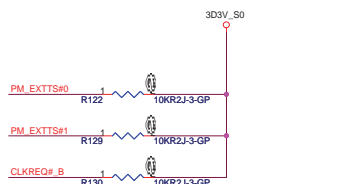
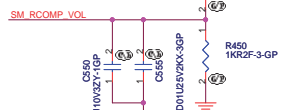
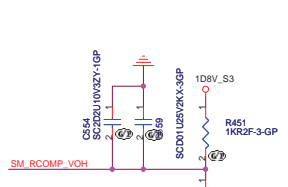
CRESTLINE-GP-U



CRESTLINE-GP-U

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Size		21F, 8B, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
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CFG[17:3] have internal pull up  
CFG[19:18] have internal pull down

From Astro demo schematic

21 PM\_BMBUS# <<< PM\_BMBUS# G41  
4,20,37 H\_DPRSTP# <<< H\_DPRSTP# 139  
15 PM\_EXTTS#0 <<< PM\_EXTTS#0 136  
16 PM\_EXTTS#1 <<< PM\_EXTTS#1 136  
PLT\_RST# <<< PLT\_RST# 19,25,31,35  
4,20,45 H\_THERMTRIP# <<< H\_THERMTRIP# N20  
21,37 DPRSLPVR <<< DPRSLPVR G36

U638 2 OF 10

X P36 RSVDP36  
X P37 RSVDP37  
X R35 RSVDP35  
X N35 RSVDP35  
X R12 RSVDP35  
X R13 RSVDP35  
X N12 RSVDP35  
X N13 RSVDP35  
X J12 RSVDP35  
X R37 RSVDP37  
X M36 RSVDP36  
X R36 RSVDP36  
X M37 RSVDP37  
X D20 RSVDP36

15 DDR\_A\_MA14 <<< DDR\_A\_MA14  
16 DDR\_B\_MA14 <<< DDR\_B\_MA14

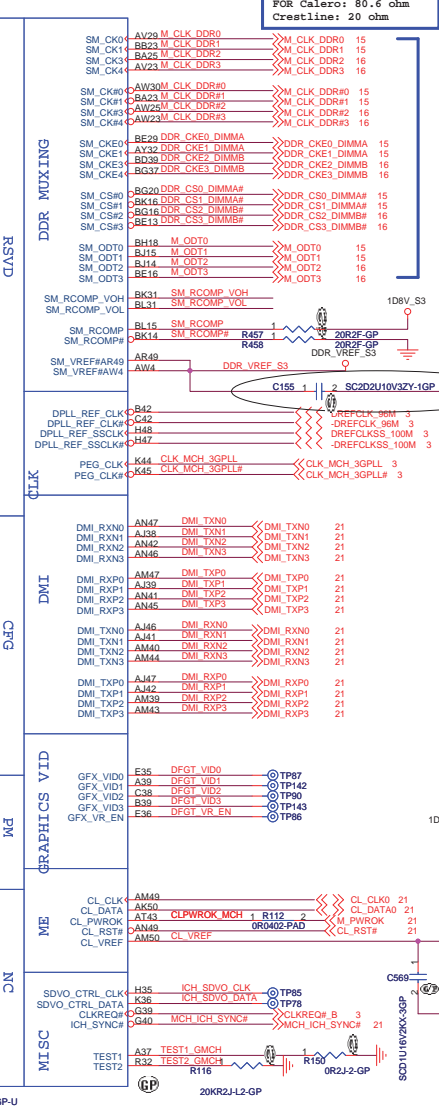
3 MCH\_CLKSEL0 <<< MCH\_CLKSEL0 P27  
3 MCH\_CLKSEL1 <<< MCH\_CLKSEL1 N27  
3 MCH\_CLKSEL2 <<< MCH\_CLKSEL2 N24

TP86 <<< CFG6 F23  
TP73 <<< CFG6 N23  
TP83 <<< CFG6 G23  
TP84 <<< CFG6 J20  
TP140 <<< CFG6 C20  
TP71 <<< CFG10 R24  
TP75 <<< CFG11 L23  
TP79 <<< CFG12 J23  
TP14 <<< CFG13 E23

TP76 <<< CFG16 M24  
TP82 <<< CFG18 L32  
TP72 <<< CFG19 N33  
TP81 <<< CFG20 L36

X J51 NCRBJ51  
X BK51 NCRBK51  
X BL50 NCRBL50  
X BL49 NCRBL49  
X BL3 NCRBL3  
X BL2 NCRBL2  
X BK1 NCRBK1  
X BL1 NCRBL1  
X E1 NCRB1  
X A5 NCRB5  
X C51 NCRB51  
X B50 NCRB50  
X A50 NCRB50  
X A49 NCRB49  
X BK2 NCRBK2

CRESTLINE-GP-U









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A13	VSS	AW24
A15	VSS	AW29
A17	VSS	AW32
A24	VSS	AW5
AA21	VSS	AW7
AA24	VSS	AY10
AA29	VSS	AY24
AB20	VSS	AY37
AB23	VSS	AY42
AB26	VSS	AY43
AB28	VSS	AY45
AB31	VSS	AY47
AC10	VSS	AY50
AC13	VSS	B10
AC3	VSS	B20
AC39	VSS	B24
AC43	VSS	B29
AC47	VSS	B30
AD1	VSS	B35
AD21	VSS	B38
AD26	VSS	B43
AD29	VSS	B46
AD3	VSS	B5
AD41	VSS	B8
AD45	VSS	BA1
AD49	VSS	BA17
AD5	VSS	BA18
AD50	VSS	BA2
AD8	VSS	BA24
AE10	VSS	BB12
AE14	VSS	BB25
AE6	VSS	BB40
AF20	VSS	BB44
AF23	VSS	BB49
AF24	VSS	BB8
AF31	VSS	BC16
AG2	VSS	BC24
AG38	VSS	BC25
AG43	VSS	BC36
AG47	VSS	BC40
AG50	VSS	J2
AH3	VSS	BC51
AH40	VSS	BD13
AH41	VSS	BD2
AH7	VSS	BD28
AH9	VSS	BD45
AJ11	VSS	BD48
AJ13	VSS	BD5
AJ21	VSS	BE1
AJ24	VSS	BE19
AJ29	VSS	BE23
AJ32	VSS	BE30
AJ43	VSS	BE42
AJ45	VSS	BE51
AJ49	VSS	BE8
AK20	VSS	BF12
AK21	VSS	BF16
AK26	VSS	BF36
AK28	VSS	BG19
AK31	VSS	BG2
AK51	VSS	BG24
AL1	VSS	BG29
AM11	VSS	BG39
AM13	VSS	BG48
AM3	VSS	BG5
AM4	VSS	BG51
AM41	VSS	BH17
AM45	VSS	BH30
AN1	VSS	BH44
AN38	VSS	BH46
AN39	VSS	BH8
AN43	VSS	BJ11
AN5	VSS	BJ13
AN7	VSS	BJ38
AP4	VSS	BJ4
AP48	VSS	BJ42
AP50	VSS	BJ46
AR11	VSS	BK15
AR2	VSS	BK17
AR39	VSS	BK25
AR44	VSS	BK29
AR47	VSS	BK36
AR7	VSS	BK40
AT10	VSS	BK44
AT14	VSS	BK6
AT41	VSS	BK8
AT49	VSS	BL11
AU1	VSS	BL13
AU23	VSS	BL19
AU29	VSS	BL22
AU3	VSS	BL37
AU36	VSS	BL47
AU49	VSS	C12
AU51	VSS	C16
AV39	VSS	C19
AV48	VSS	C28
AW1	VSS	C29
AW12	VSS	C33
AW16	VSS	C36
	VSS	C41

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C46	VSS	W11
C50	VSS	W39
C7	VSS	W43
D13	VSS	W47
D24	VSS	W5
D3	VSS	W7
D324	VSS	Y13
D39	VSS	Y2
D45	VSS	Y41
D49	VSS	Y45
E10	VSS	Y49
E16	VSS	Y5
E24	VSS	Y50
E28	VSS	Y11
E32	VSS	P29
E47	VSS	T29
F19	VSS	T31
F36	VSS	T33
F4	VSS	R28
F40	VSS	
F50	VSS	
G1	VSS	
G13	VSS	
G16	VSS	AA32
G19	VSS	AB32
G24	VSS	AB32
G28	VSS	AF28
G29	VSS	AF29
G33	VSS	AT27
G42	VSS	AV25
G45	VSS	H50
G48	VSS	
GB44	VSS	
H24	VSS	
H28	VSS	
H4	VSS	
H45	VSS	
J11	VSS	
J16	VSS	
J2	VSS	
J24	VSS	
J28	VSS	
J33	VSS	
J35	VSS	
J39	VSS	
K12	VSS	
K47	VSS	
K8	VSS	
L1	VSS	
L17	VSS	
L20	VSS	
L24	VSS	
L28	VSS	
L3	VSS	
L33	VSS	
L49	VSS	
M28	VSS	
M42	VSS	
M46	VSS	
M49	VSS	
M5	VSS	
M50	VSS	
M9	VSS	
N11	VSS	
N14	VSS	
N17	VSS	
N29	VSS	
N32	VSS	
N36	VSS	
N39	VSS	
N44	VSS	
N49	VSS	
N7	VSS	
P19	VSS	
P2	VSS	
P23	VSS	
P3	VSS	
P50	VSS	
R49	VSS	
T39	VSS	
T43	VSS	
T47	VSS	
U41	VSS	
U45	VSS	
U50	VSS	
V2	VSS	
V3	VSS	

VSS

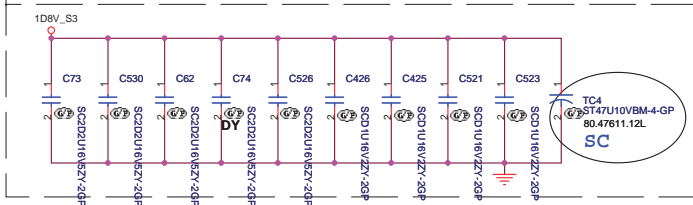
CRESTLINE-GP-U



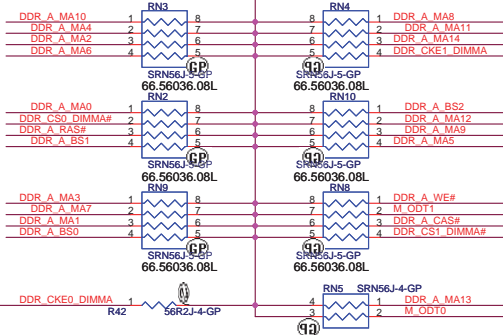
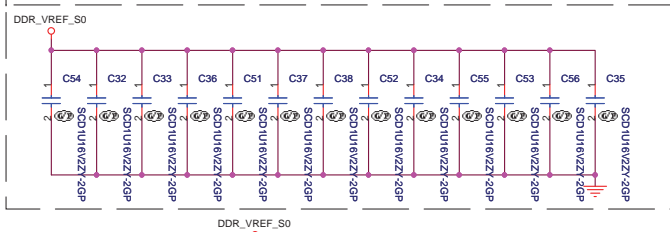
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Title		Wistron Corporation	
Size		21F, 8B, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
A3		CRESTLINE(6/6)-PWR/GND	
Date: Friday, March 09, 2007		F-note 2.0	
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Rev		SC	

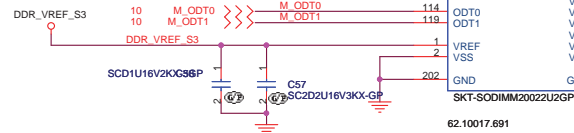
Layout Note:  
Place near DM1



Layout Note:  
Place one cap close to every 2 pullup resistors terminated to +0.9V5



Layout Note:  
Place these resistors  
closely DM1, all  
trace length Max=1.5"



DDR_A_MA0	102	DM2	108	DDR_A_RAS#	9
DDR_A_MA1	101	A1	109	DDR_A_WE#	9
DDR_A_MA2	100	A2	113	DDR_A_CAS#	9
DDR_A_MA3	99	A3			
DDR_A_MA4	98	A4	110	DDR_CS0_DIMMA#	10
DDR_A_MA5	97	A5	115	DDR_CS1_DIMMA#	10
DDR_A_MA6	96	A6			
DDR_A_MA7	95	A7	79	DDR_CKE0_DIMMA	10
DDR_A_MA8	94	A8	80	DDR_CKE1_DIMMA	10
DDR_A_MA9	93	A9			
DDR_A_MA10	92	A10/AP	30	M_CLK_DDR0	10
DDR_A_MA11	91	A11	32	M_CLK_DDR#0	10
DDR_A_MA12	90	A12			
DDR_A_MA13	89	A13	164	M_CLK_DDR1	10
DDR_A_MA14	88	A14	166	M_CLK_DDR#1	10
DDR_A_BS2	87	A15			
DDR_A_BS0	86	A16/BA2			
DDR_A_BS1	85	BA0			
DDR_A_D0	84	BA1			
DDR_A_D1	83	DQ0			
DDR_A_D2	82	DQ1			
DDR_A_D3	81	DQ2			
DDR_A_D4	80	DQ3			
DDR_A_D5	79	DQ4			
DDR_A_D6	78	DQ5			
DDR_A_D7	77	DQ6			
DDR_A_D8	76	DQ7			
DDR_A_D9	75	DQ8			
DDR_A_D10	74	DQ9			
DDR_A_D11	73	DQ10			
DDR_A_D12	72	DQ11			
DDR_A_D13	71	DQ12			
DDR_A_D14	70	DQ13			
DDR_A_D15	69	DQ14			
DDR_A_D16	68	DQ15			
DDR_A_D17	67	DQ16			
DDR_A_D18	66	DQ17			
DDR_A_D19	65	DQ18			
DDR_A_D20	64	DQ19			
DDR_A_D21	63	DQ20			
DDR_A_D22	62	DQ21			
DDR_A_D23	61	DQ22			
DDR_A_D24	60	DQ23			
DDR_A_D25	59	DQ24			
DDR_A_D26	58	DQ25			
DDR_A_D27	57	DQ26			
DDR_A_D28	56	DQ27			
DDR_A_D29	55	DQ28			
DDR_A_D30	54	DQ29			
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DDR_A_D32	52	DQ31			
DDR_A_D33	51	DQ32			
DDR_A_D34	50	DQ33			
DDR_A_D35	49	DQ34			
DDR_A_D36	48	DQ35			
DDR_A_D37	47	DQ36			
DDR_A_D38	46	DQ37			
DDR_A_D39	45	DQ38			
DDR_A_D40	44	DQ39			
DDR_A_D41	43	DQ40			
DDR_A_D42	42	DQ41			
DDR_A_D43	41	DQ42			
DDR_A_D44	40	DQ43			
DDR_A_D45	39	DQ44			
DDR_A_D46	38	DQ45			
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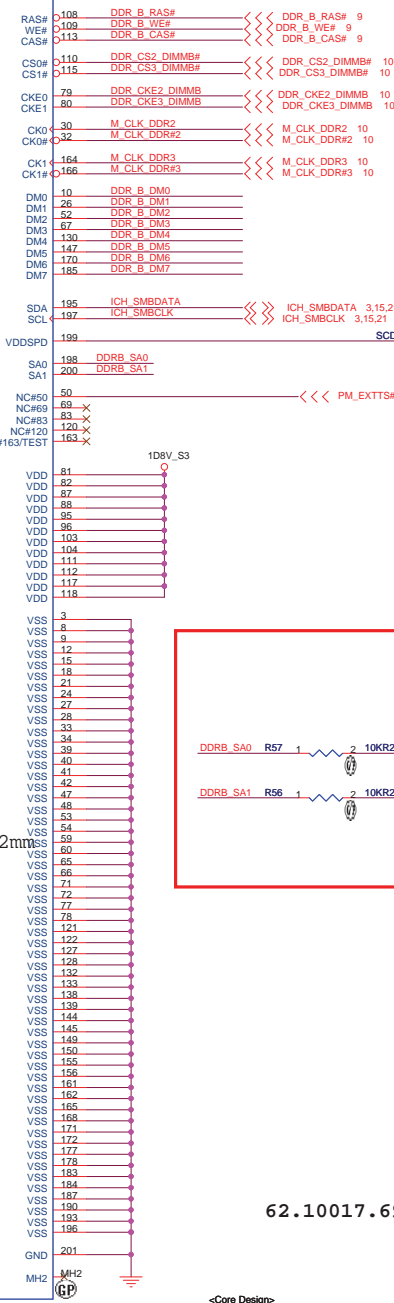
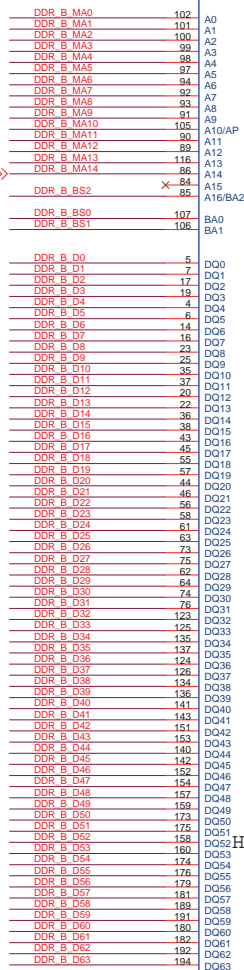
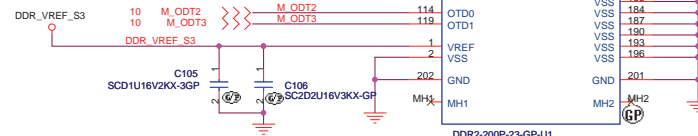
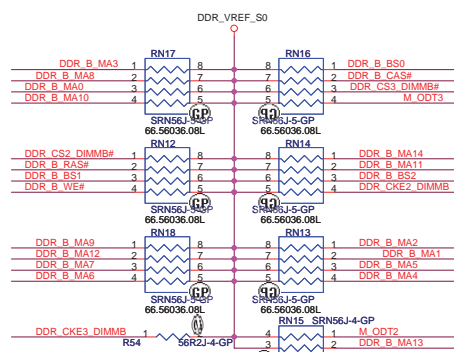
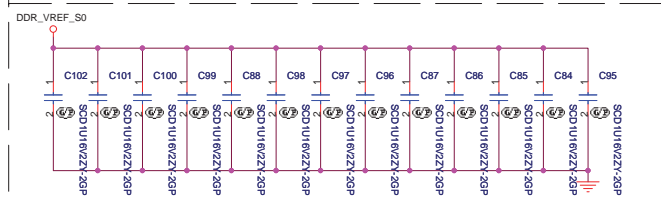
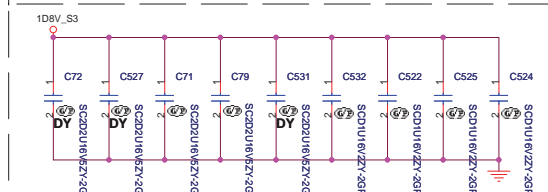
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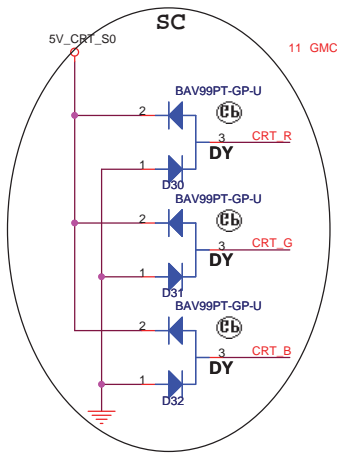
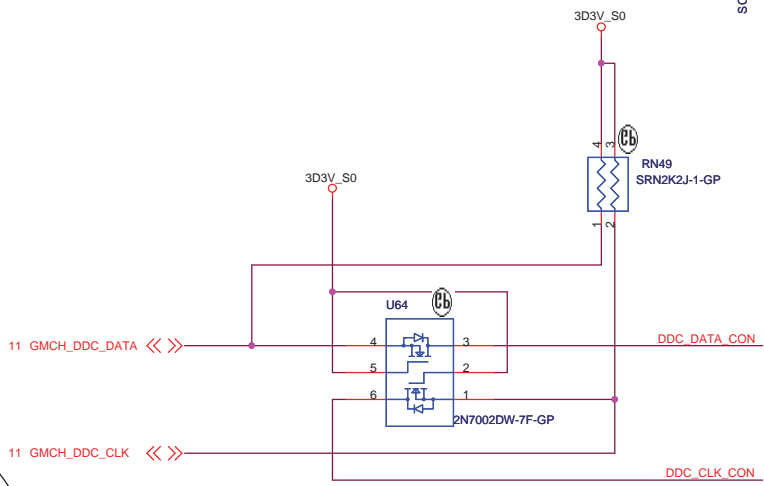
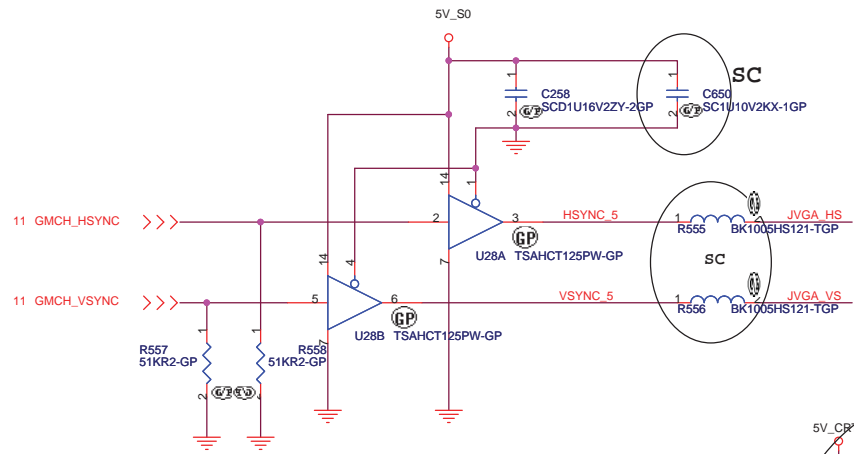
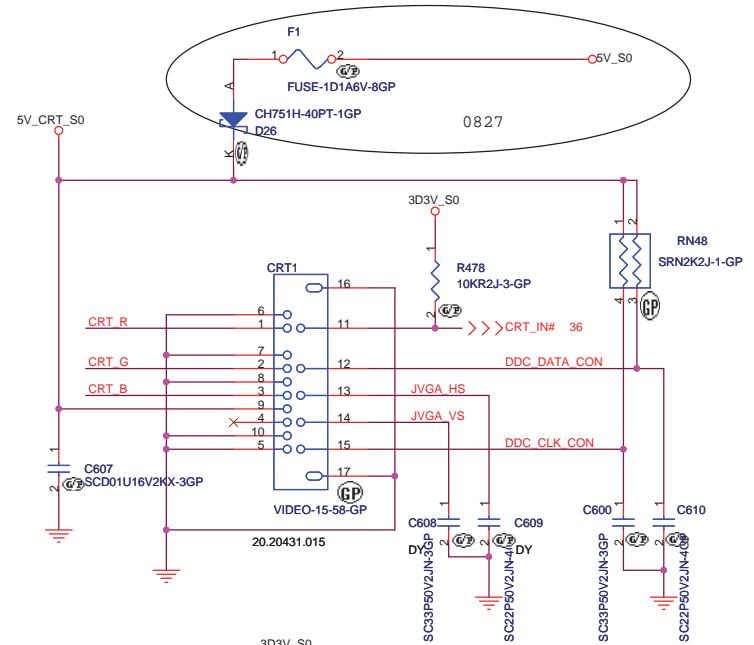
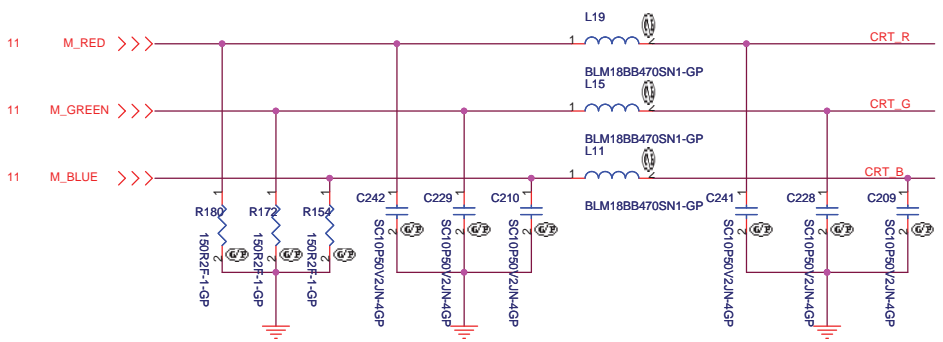
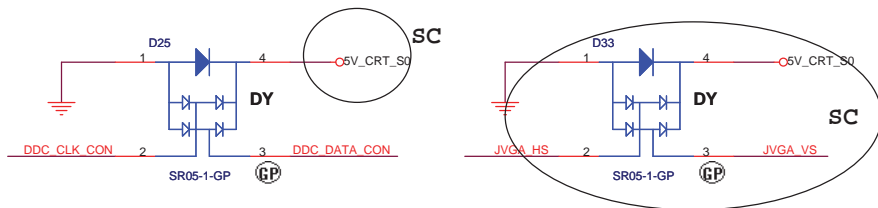
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21F, 88, Sec.1, Hsin Tai Wu Rd., Heichih,  
Taipai Hsien 221, Taiwan, R.O.C.

File		
DDR2-SODIMM SLOT1		
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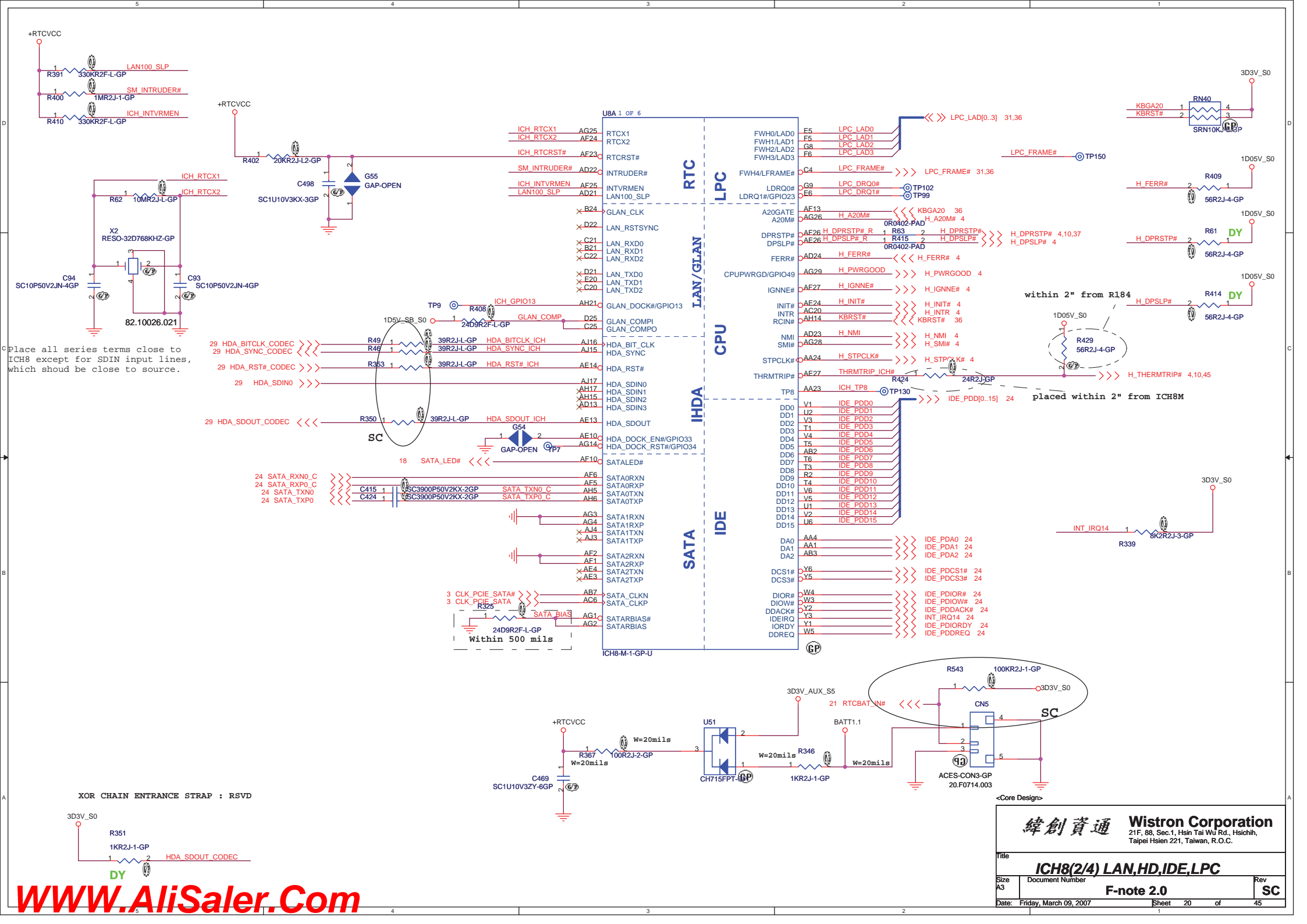




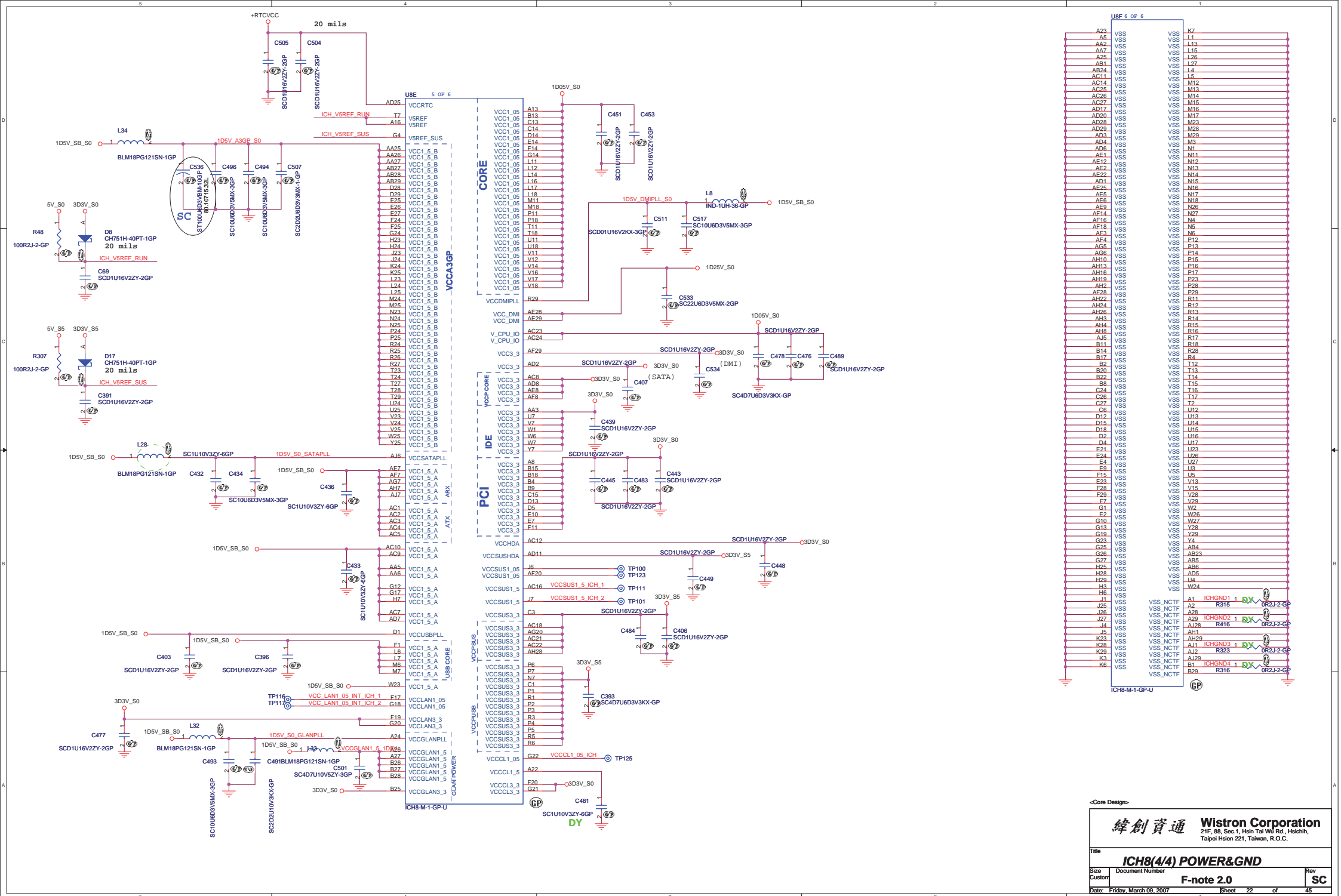
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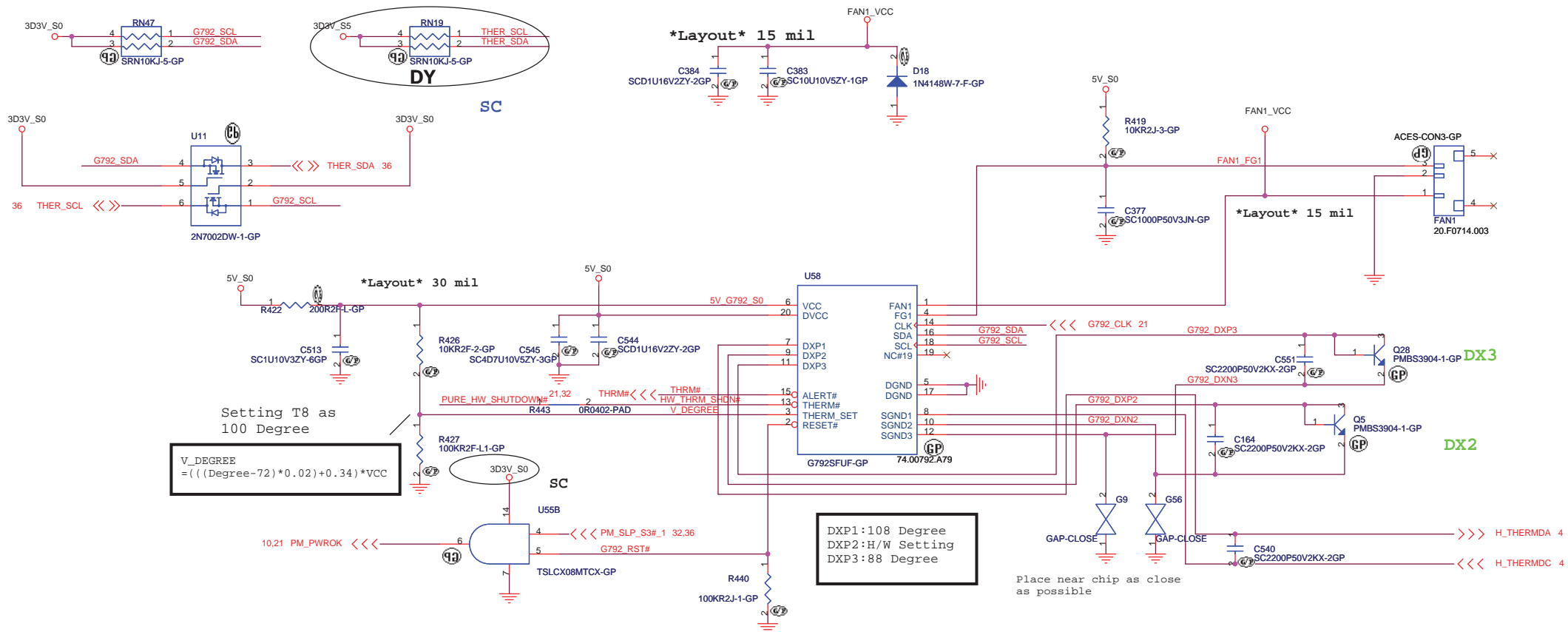
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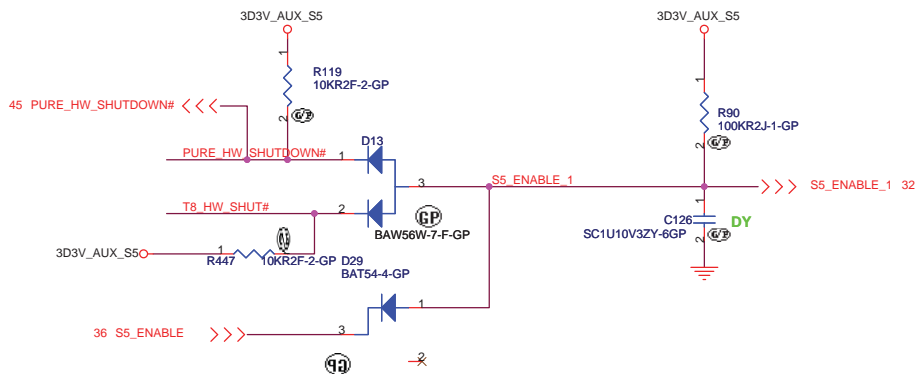
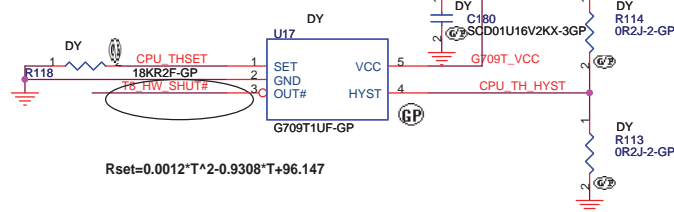






### Dummy when G792 enhanced T8 function

HW thermal shut down temperature setting 95 degree . Put Near CPU .

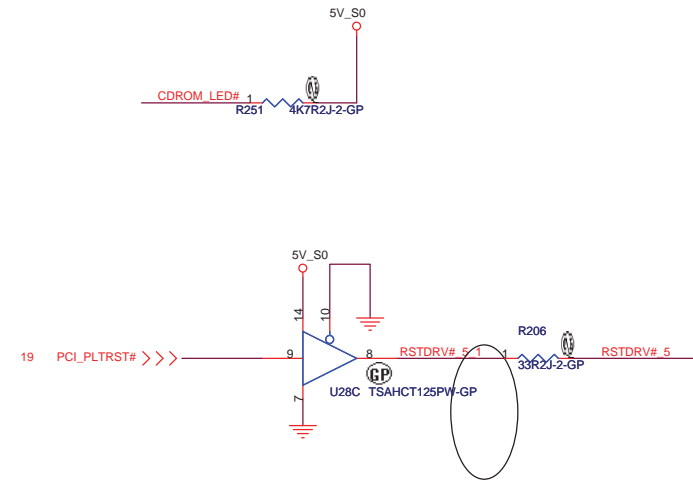


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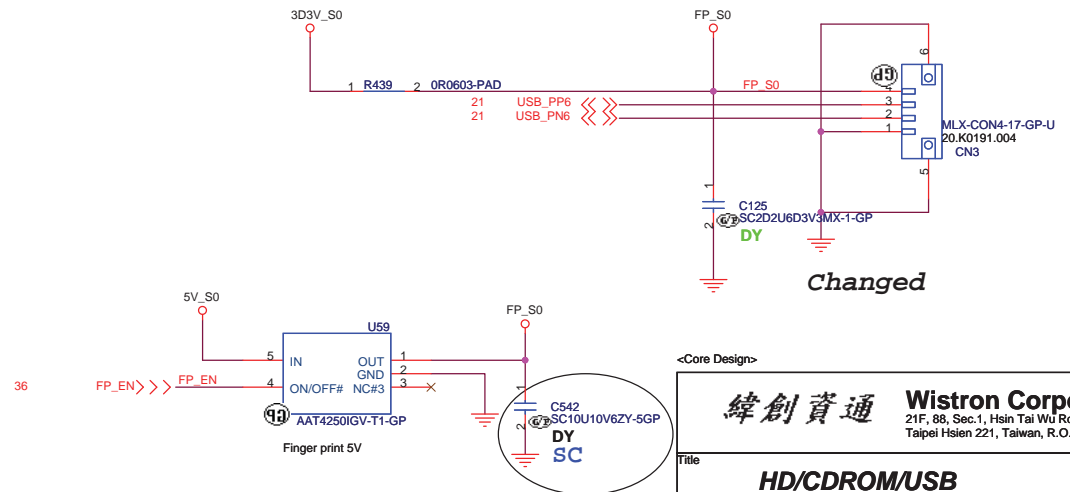
**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

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Size	Document Number	F-note 2.0	
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Date:	Friday, March 09, 2007	Sheet	23 of 45

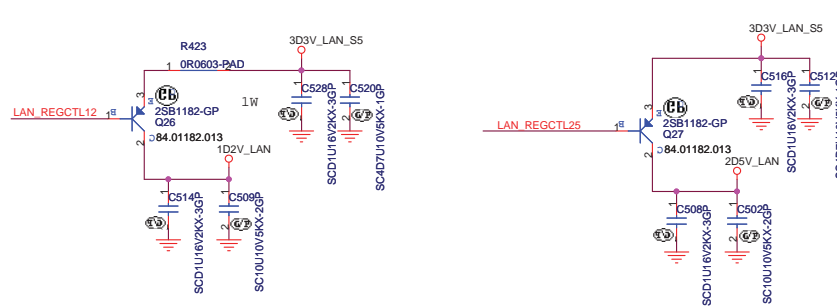
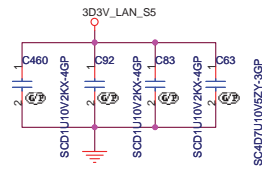
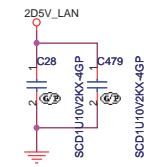
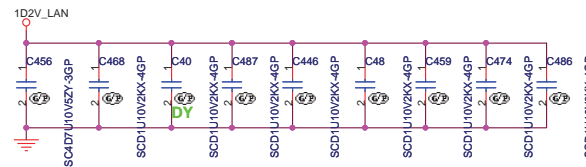
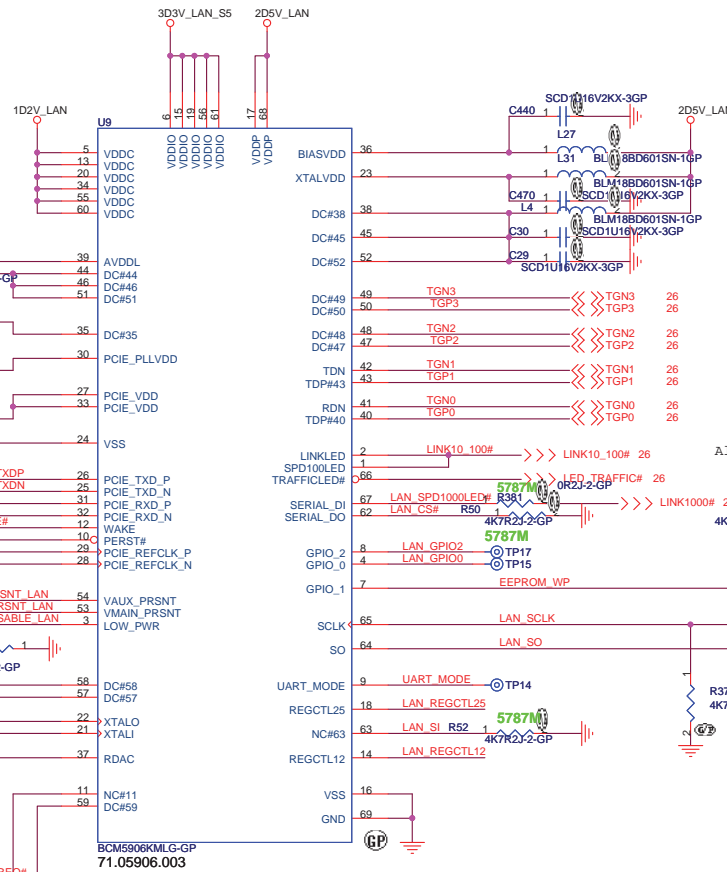
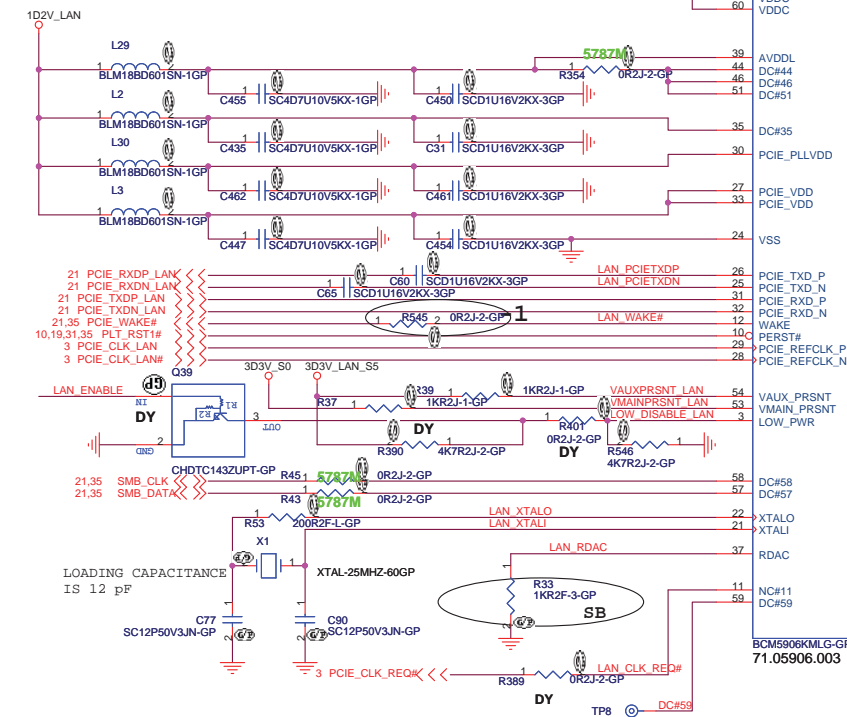
**VWW.AliSaler.Com**



## Finger Print



Don't install terminations for 5787m . 5787m  
already has integrated them inside (R669,R667,  
R212,R136,C890,C883)



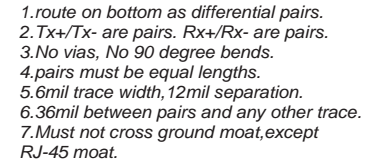
2 Kbit Electrically Erasable PROM.  
Note: For high density EEPROM 32Kbit  
-512Kbit, Remove R764

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緯創資通

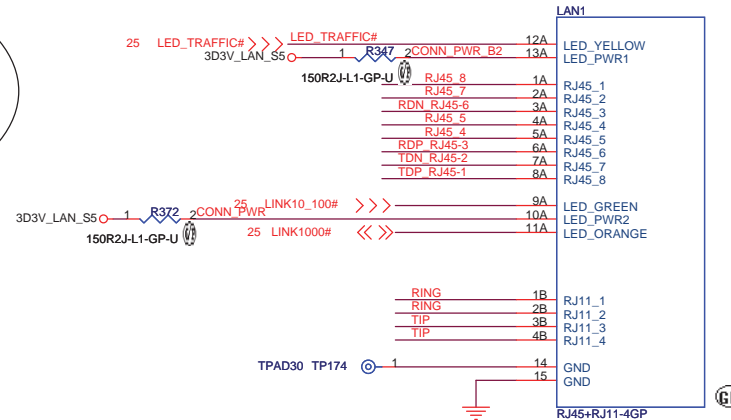
**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title			
<b>BROADCOM LAN</b>			
Size Custom	Document Number		Rev
	<b>F-note 2.0</b>		<b>SC</b>
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The diagram shows the SB module with the following connections:

- 3D3V\_LAN\_S5** is connected to the top of the **R356** resistor.
- The bottom of **R356** is connected to the **LED\_TRAFFIC#** signal line.
- The **LED\_TRAFFIC#** signal line is connected to the **10KR2J-3-GP** component.
- The **LED\_TRAFFIC#** signal line is also connected to the **LINK10\_100#** signal line.
- The **LINK10\_100#** signal line is connected to the **10KR2J-3-GP** component.
- The **LINK1000#** signal line is connected to the **10KR2J-3-GP** component.
- The **10KR2J-3-GP** component is connected to the **R360** resistor.
- The bottom of **R360** is connected to the **LINK1000#** signal line.



- <Core Design>

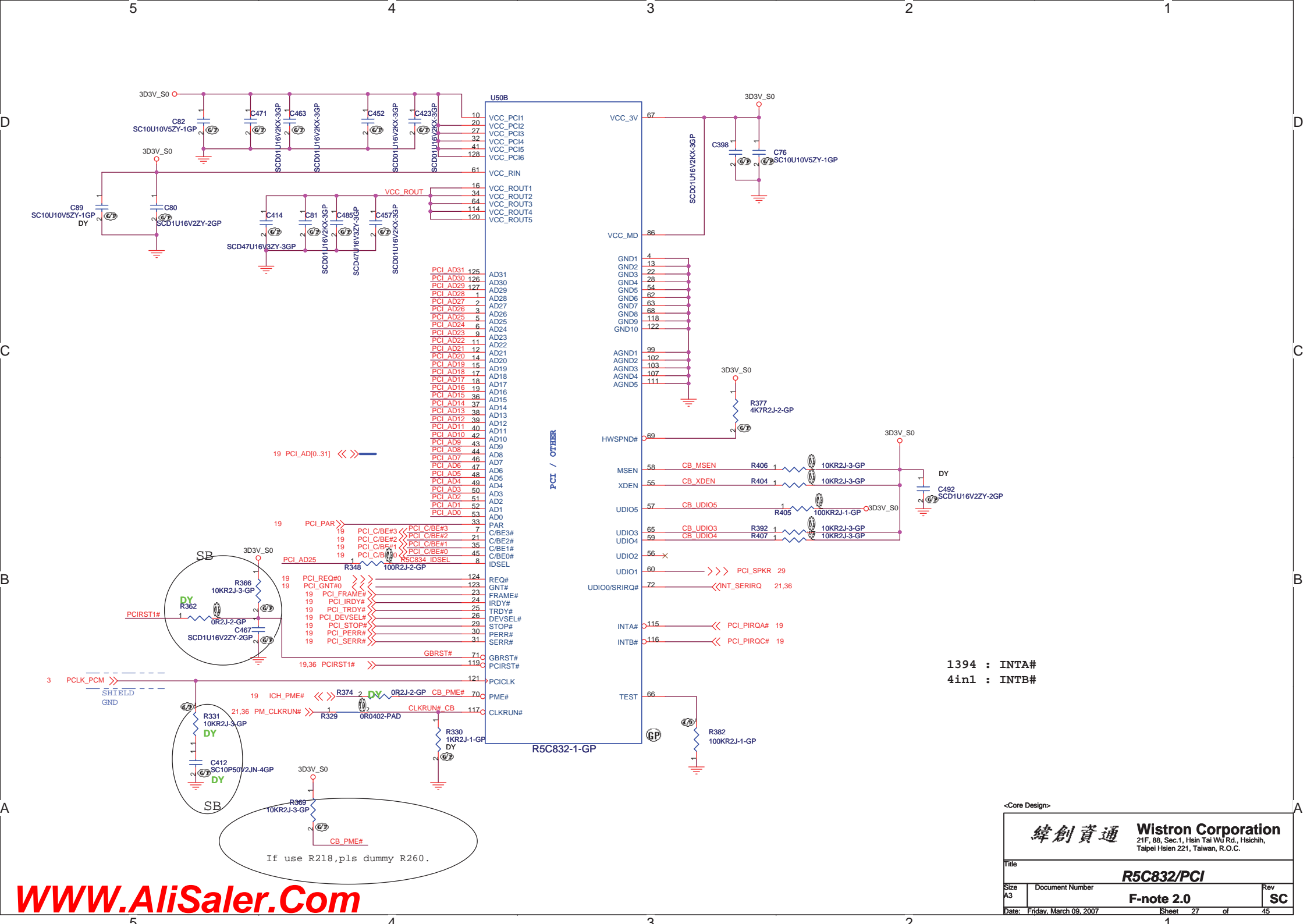
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Taipei Hsien 221, Taiwan, R.O.C.

Rev  
**SC**

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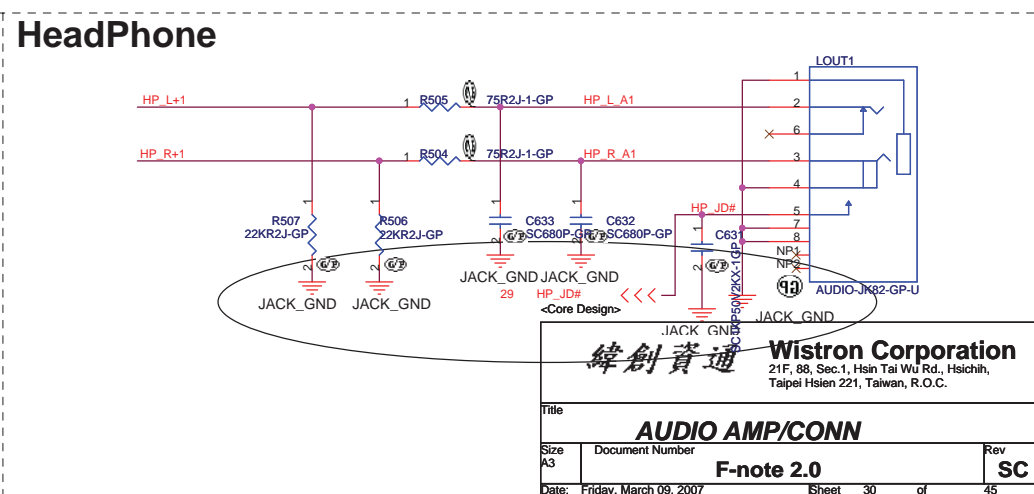
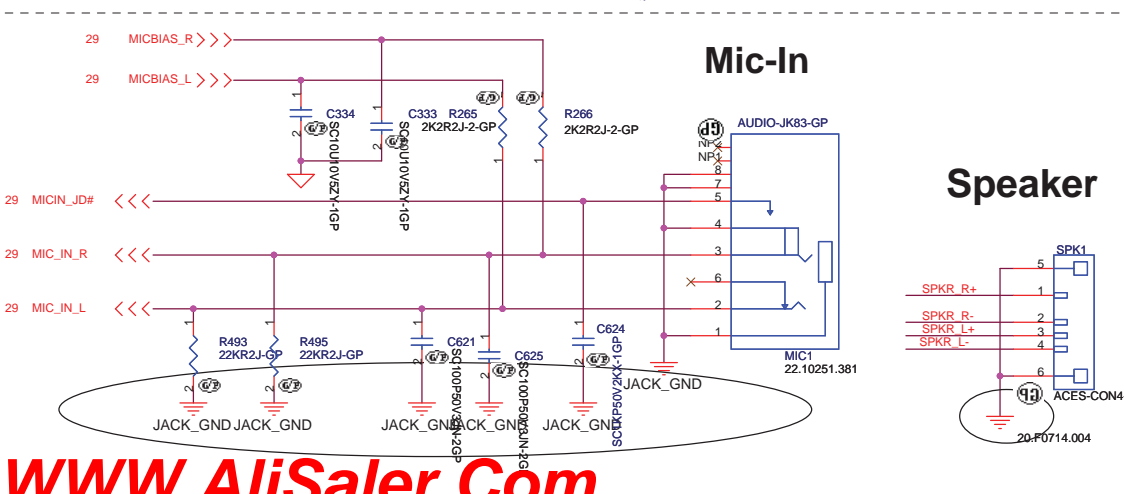
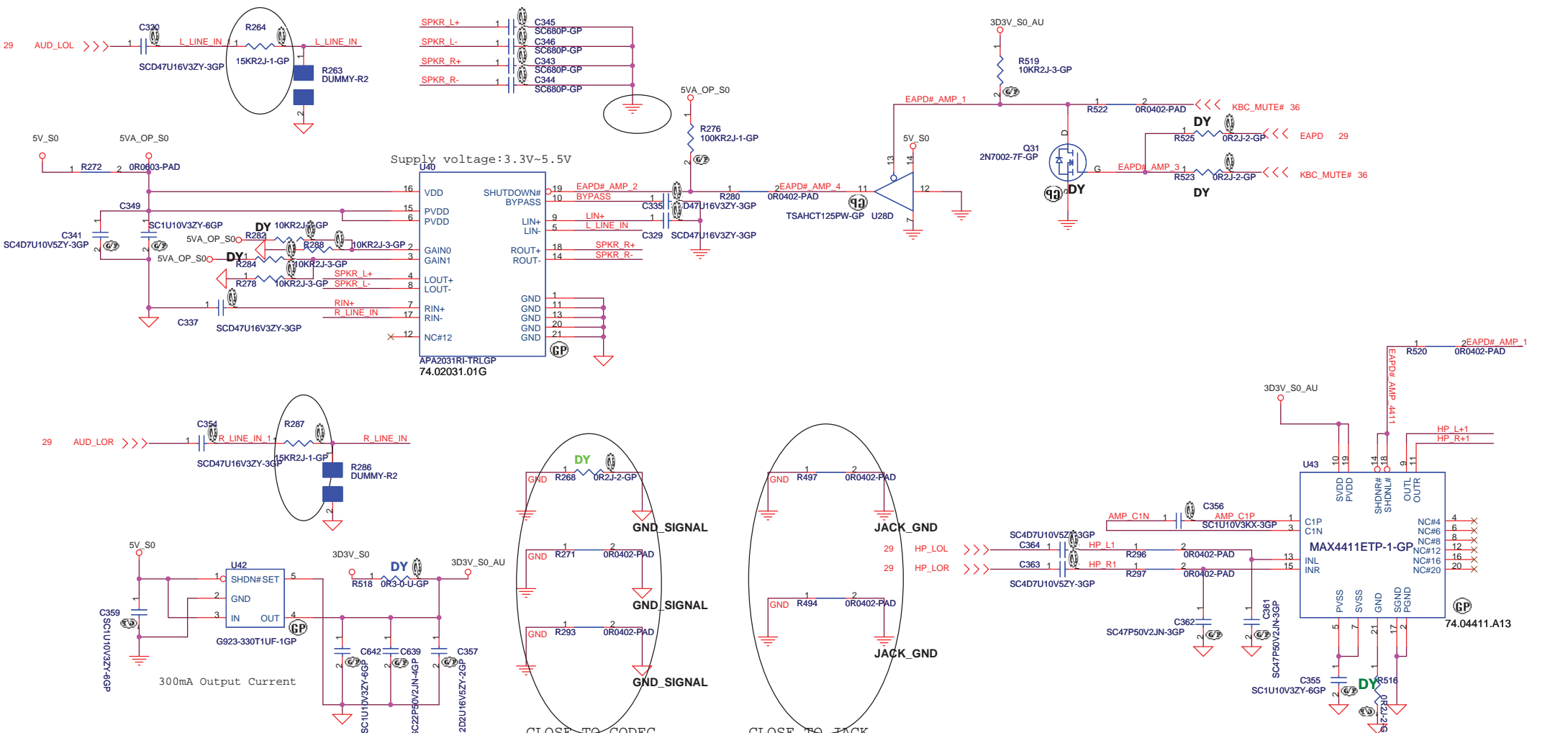
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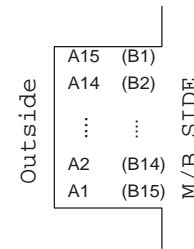








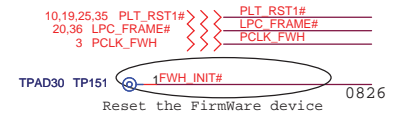
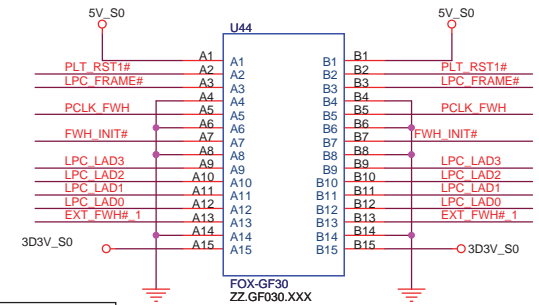
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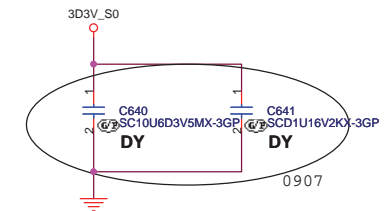
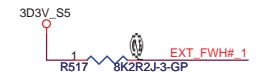
# (BOTTOM VIEW)

Boot Device must have ID[3:0] = 0000  
Has internal pull-down resistors  
All may be left floated  
FPET7 Elec. P3-46

# GOLDEN FINGER FOR DEBUG BOARD



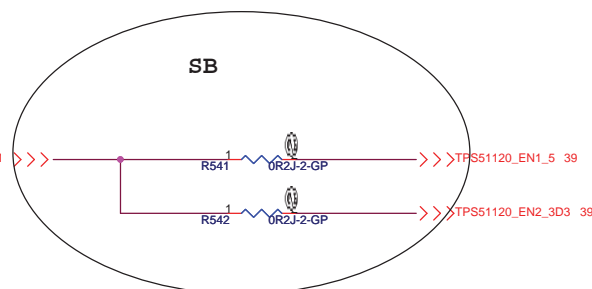
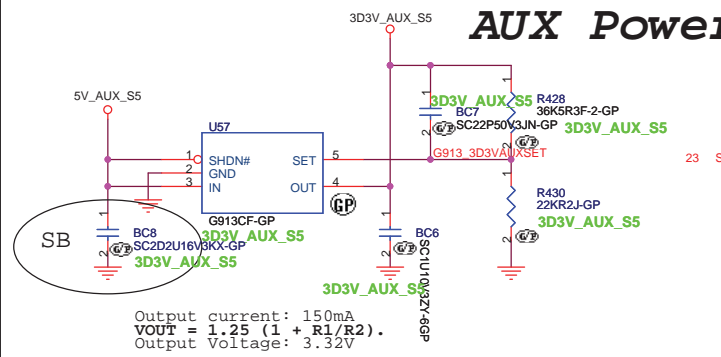
Put near board edge



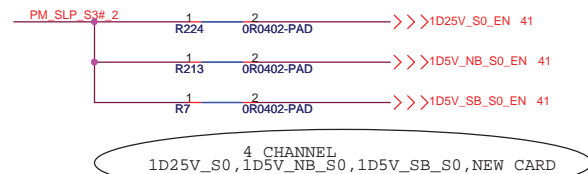
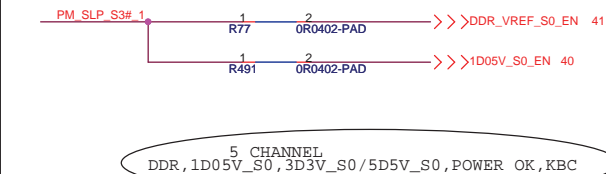
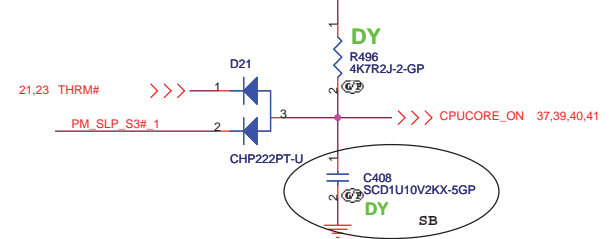
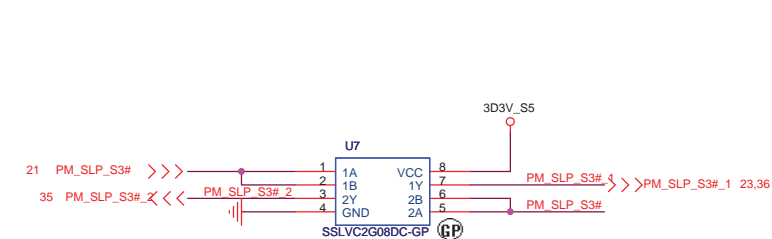
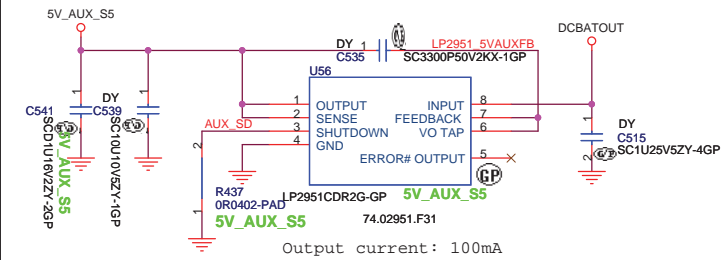
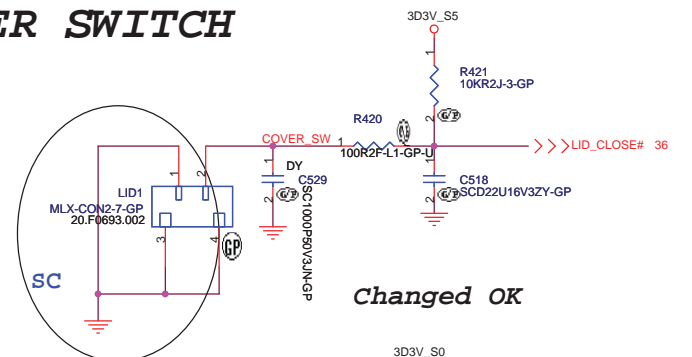
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Title	
<b>FWH and Debug</b>	
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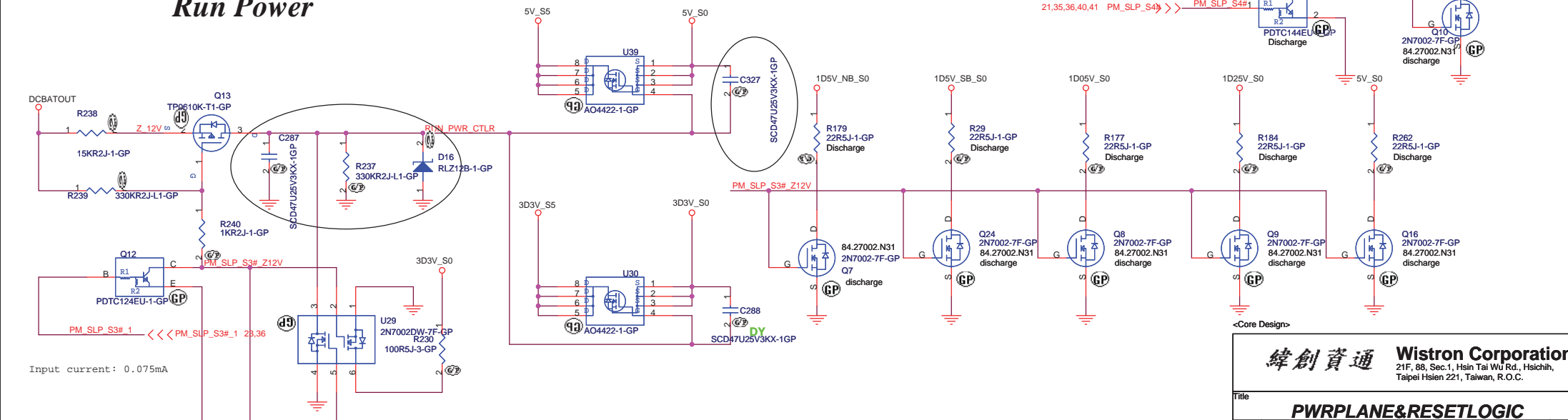
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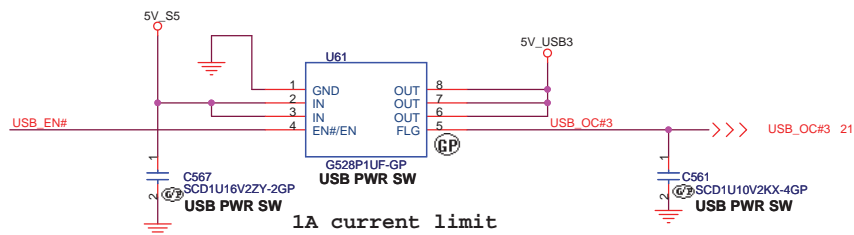
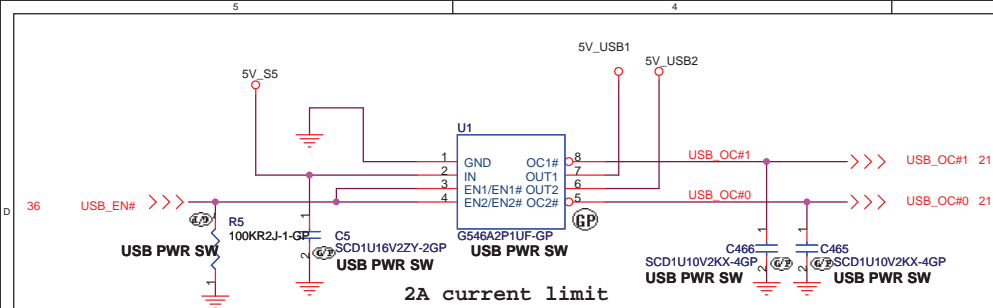


## COVER SWITCH

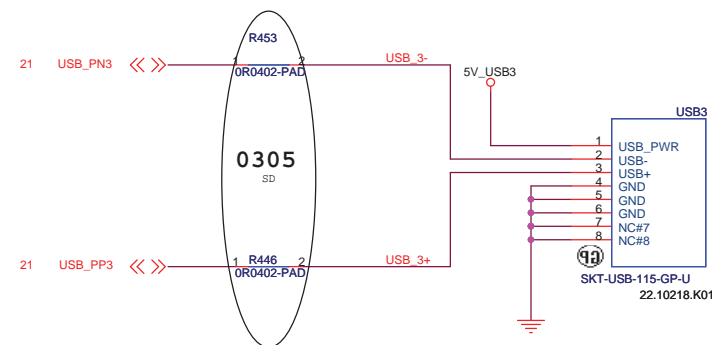
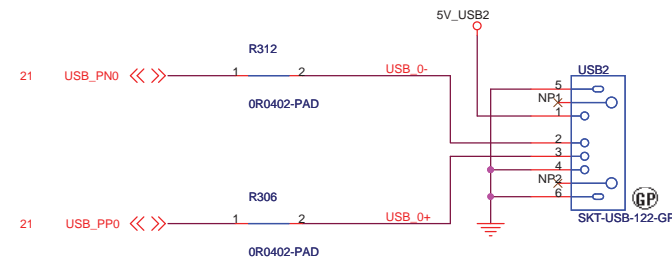
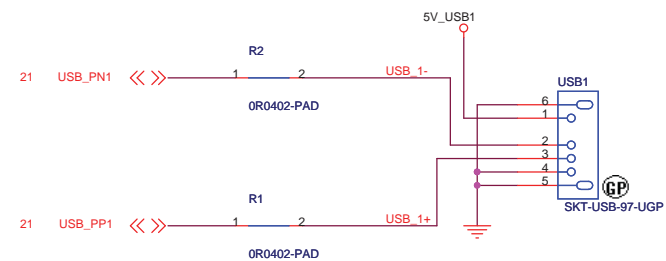


## Run Power

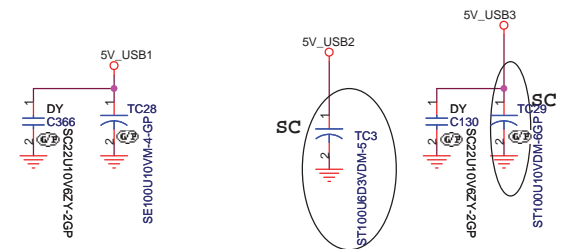
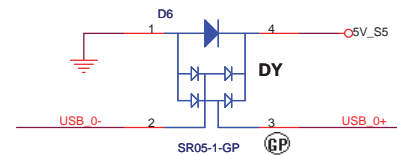
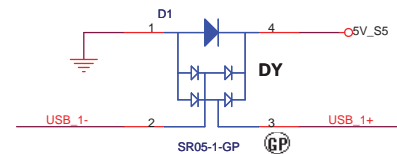
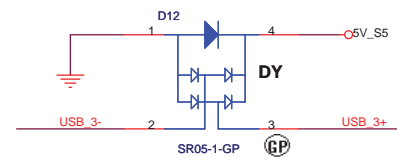
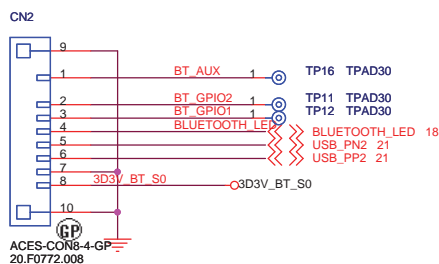
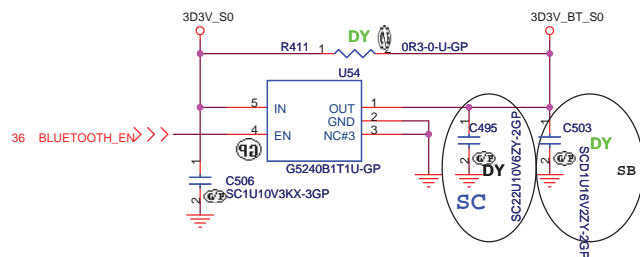




## USB CONN



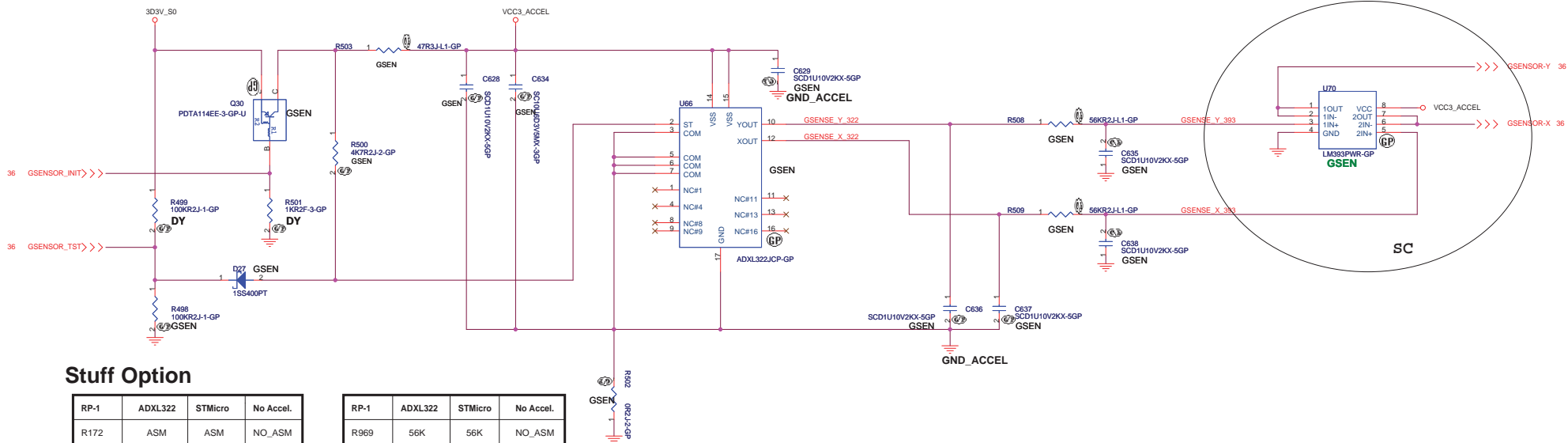
## BlueTooth



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Title		Clock generator CY28548	
Size	Document Number	F-note 2.0	
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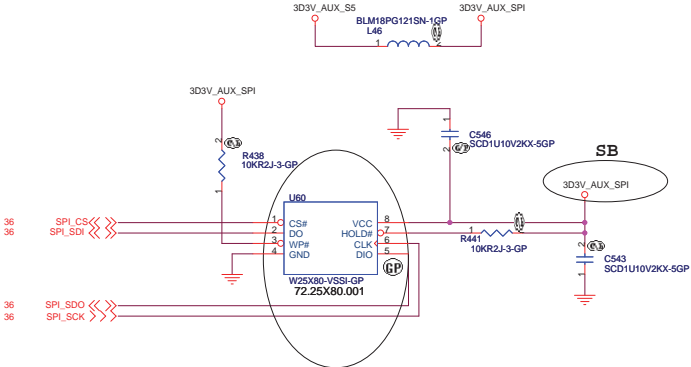


# Stuff Option

RP-1	ADXL322	STMicro	No Accel.
R172	ASM	ASM	NO_ASM
R173	ASM	ASM	NO_ASM
U9	NO_ASM	LIS2L02AL	NO_ASM
Q105	ASM	ASM	NO_ASM
D97	ASM	ASM	NO_ASM
R956	NO_ASM	ASM	NO_ASM
R62	ASM	ASM	NO_ASM
R885	10 Ohm	10 Ohm	NO_ASM
C829	ASM	ASM	NO_ASM
C969	ASM	ASM	NO_ASM
R959	ASM	ASM	NO_ASM
C830	NO_ASM	0.033UF	NO_ASM
C847	NO_ASM	0.033UF	NO_ASM

RP-1	ADXL322	STMicro	No Accel.
R969	56K	56K	NO_ASM
C938	ASM	ASM	NO_ASM
R970	56K	56K	NO_ASM
C956	ASM	ASM	NO_ASM
U66	ADXL322	NO_ASM	NO_ASM
C170	ASM	NO_ASM	NO_ASM
C178	ASM	NO_ASM	NO_ASM
C190	ASM	NO_ASM	NO_ASM
R31	ASM	NO_ASM	NO_ASM

# SPI ROM for System & KBC



- WINBOND W25X80
- SST 25VF080B

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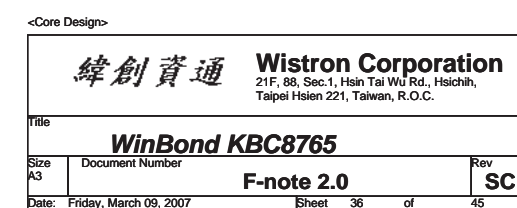


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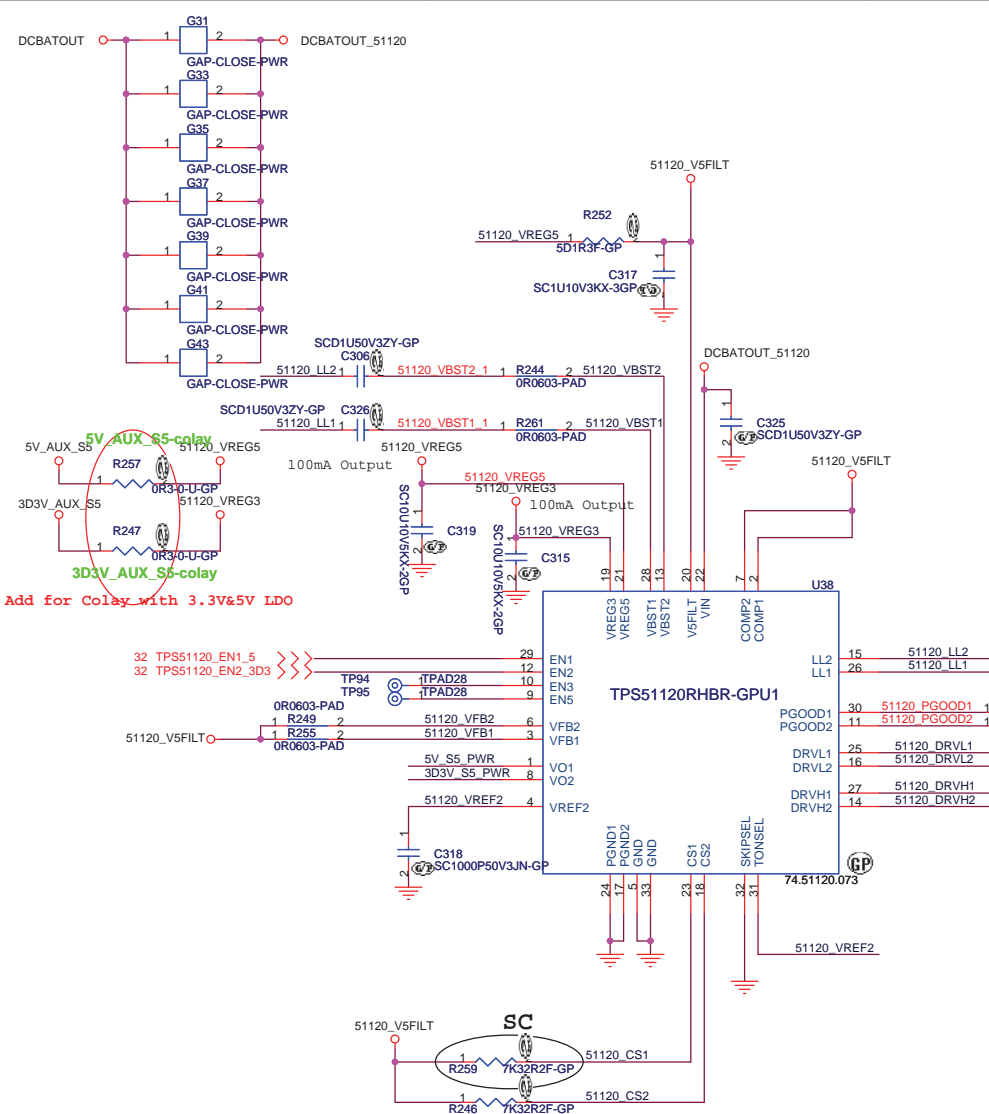
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Taipei Hsien 221, Taiwan, R.O.C.

Title			
<b>MINI CARD/NEWCARD CONN</b>			
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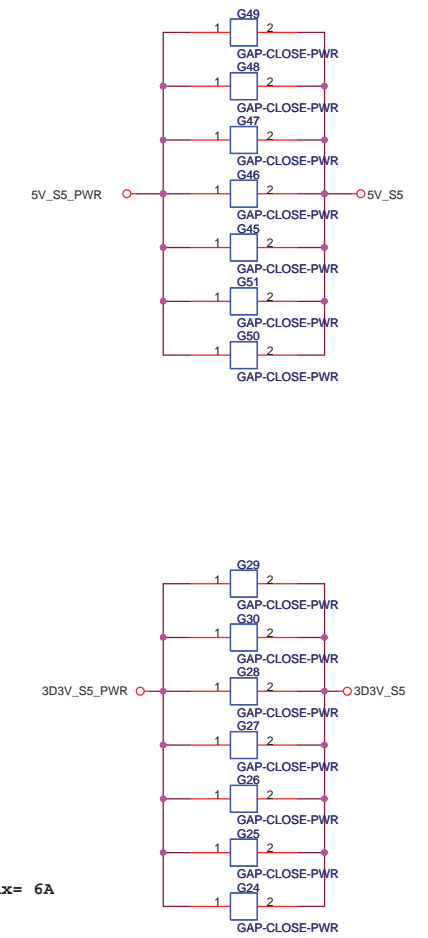
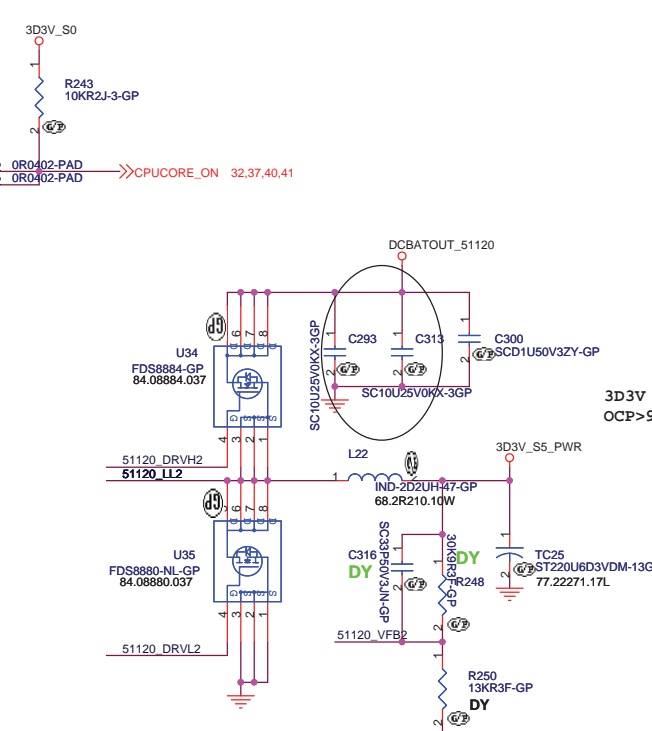
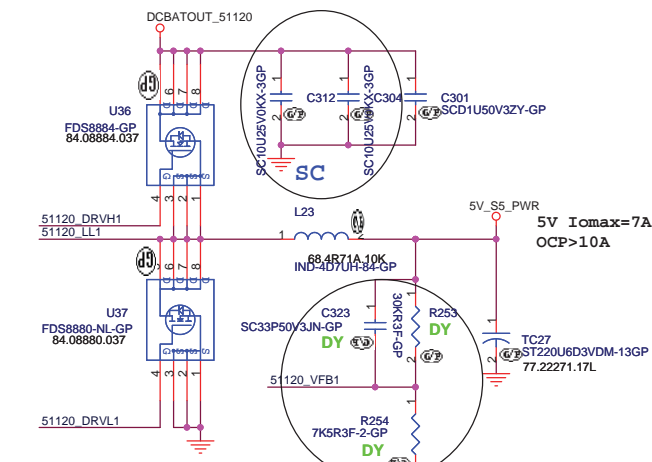
	GND	VREF2	FLOAT	V5FILT
SKIPSEL	AUTOSKIP	AUTOSKIP / FAULTS OFF	PWM	PWM
	N/A	N/A	CURRENT MODE	D-Cap MODE
	380k/CH1 590k/CH2	280k/CH1 430k/CH2	220k/CH1 330k/CH2	180k/CH1 280k/CH2
	N/A	not use	ADJ.	5V Fixed Output
	N/A	not use	ADJ.	3.3V Fixed Output
	switcher OFF	not use	Switchchr ON	Switcher ON
	not use	not use	LDO ON	REG3 on

For TPS51120,  
Vout=5V

1. If you use a 6.8uH inductor, the minimum ESR is 70m ohm.
2. If you use a 4.7uH inductor, the minimum ESR is 48m ohm.
3. If you use a 3.3uH inductor, the minimum ESR is 34m ohm.

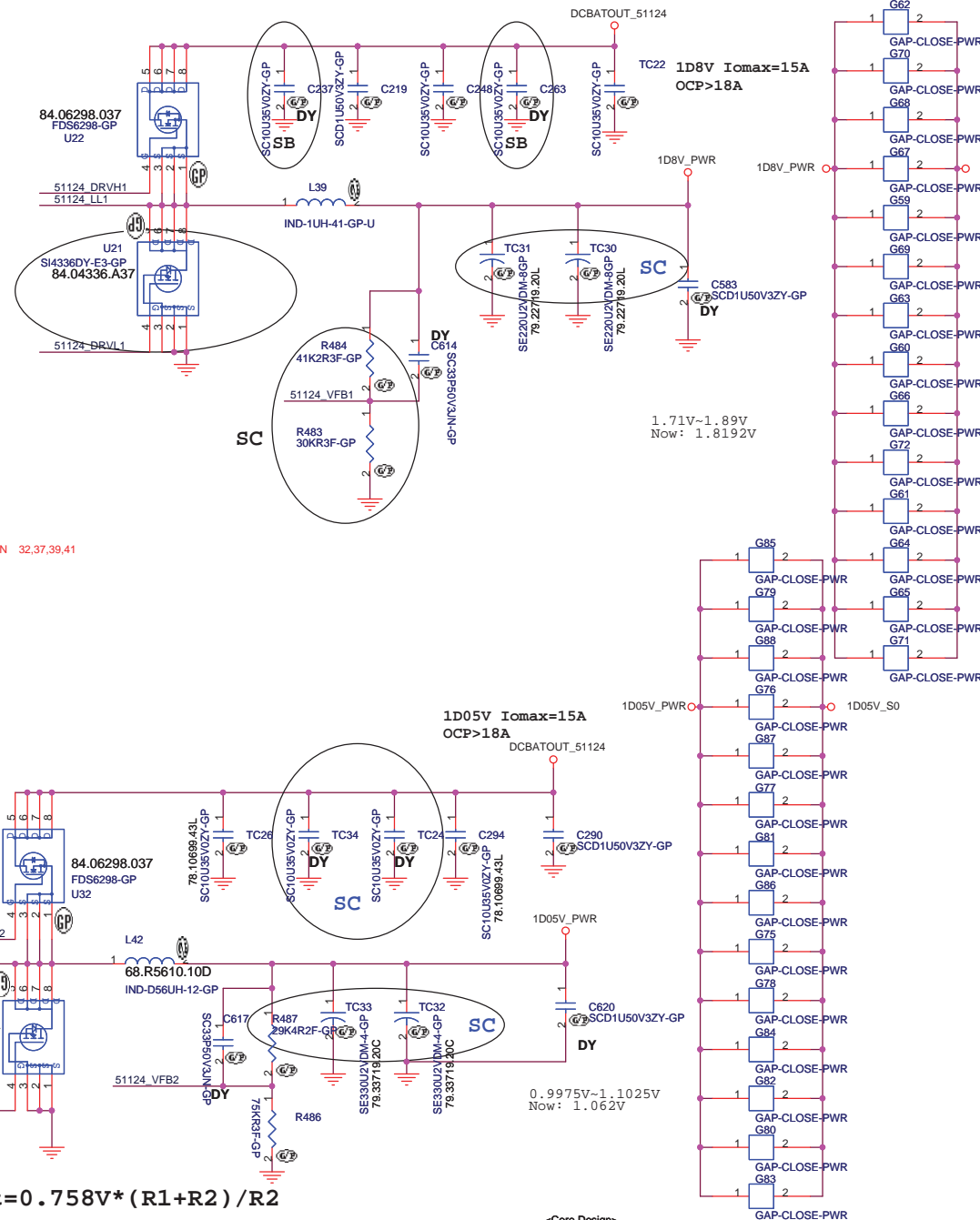
Vout=3.3V

1. If you use a 4.7uH inductor, the minimum ESR is 51m ohm.
2. If you use a 3.3uH inductor, the minimum ESR is 36m ohm.
3. If you use a 2.5uH inductor, the minimum ESR is 27m ohm.



	GND	OPEN	V5FILT
TONSEL	230k/CH1 283k/CH2	283k/CH1 346k/CH2	360k/CH1 420k/CH2

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$$V_{out} = 0.758V * (R1 + R2) / R2$$

$$I_{ocp} = (V_{trip}/R_{dson}) + ((1/(2*L*f)) * ((V_{in} - V_{out}) * V_{out}) / V_{in}))$$

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Title

**TPS51124 1D8V 1D05V**

Size

Document Number	
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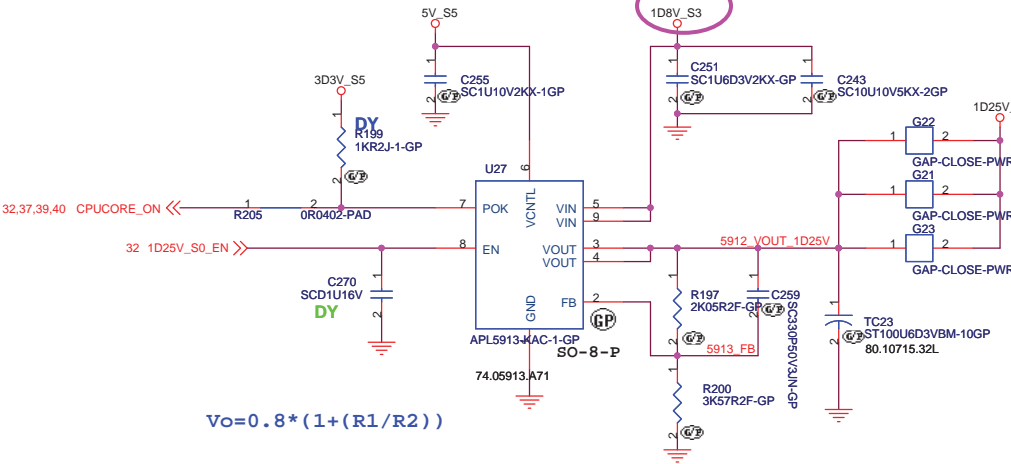
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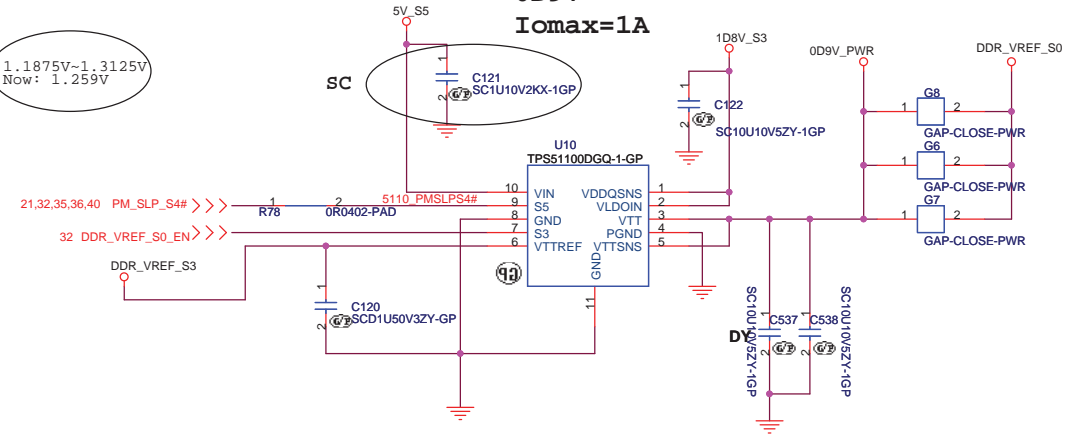
# 1D25V\_S0 Iomax=2A

Modify it

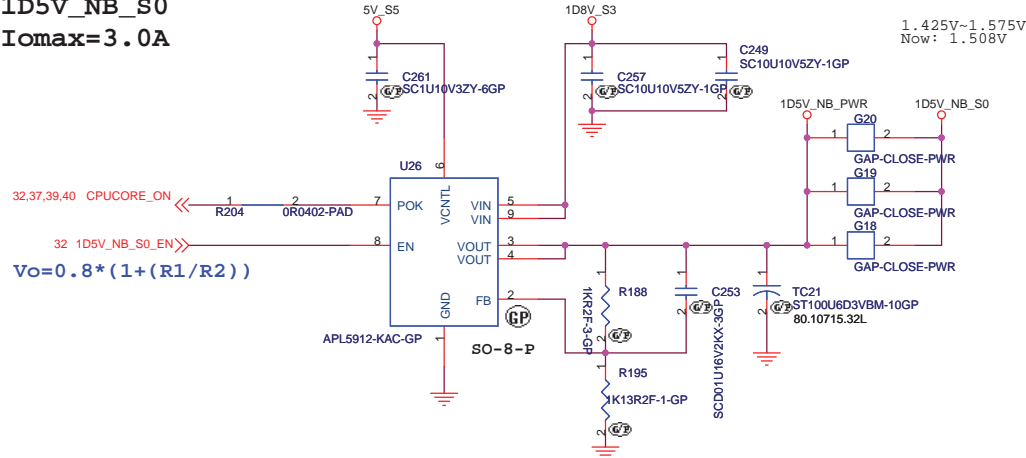


# 0D9V Iomax=1A

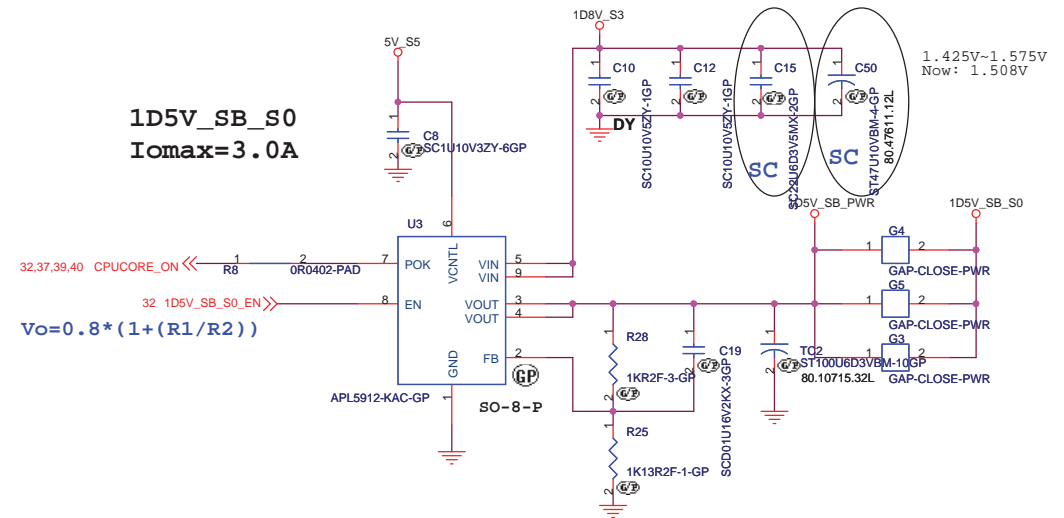
1.1875V~1.3125V  
Now: 1.259V



# 1D5V\_NB\_S0 Iomax=3.0A



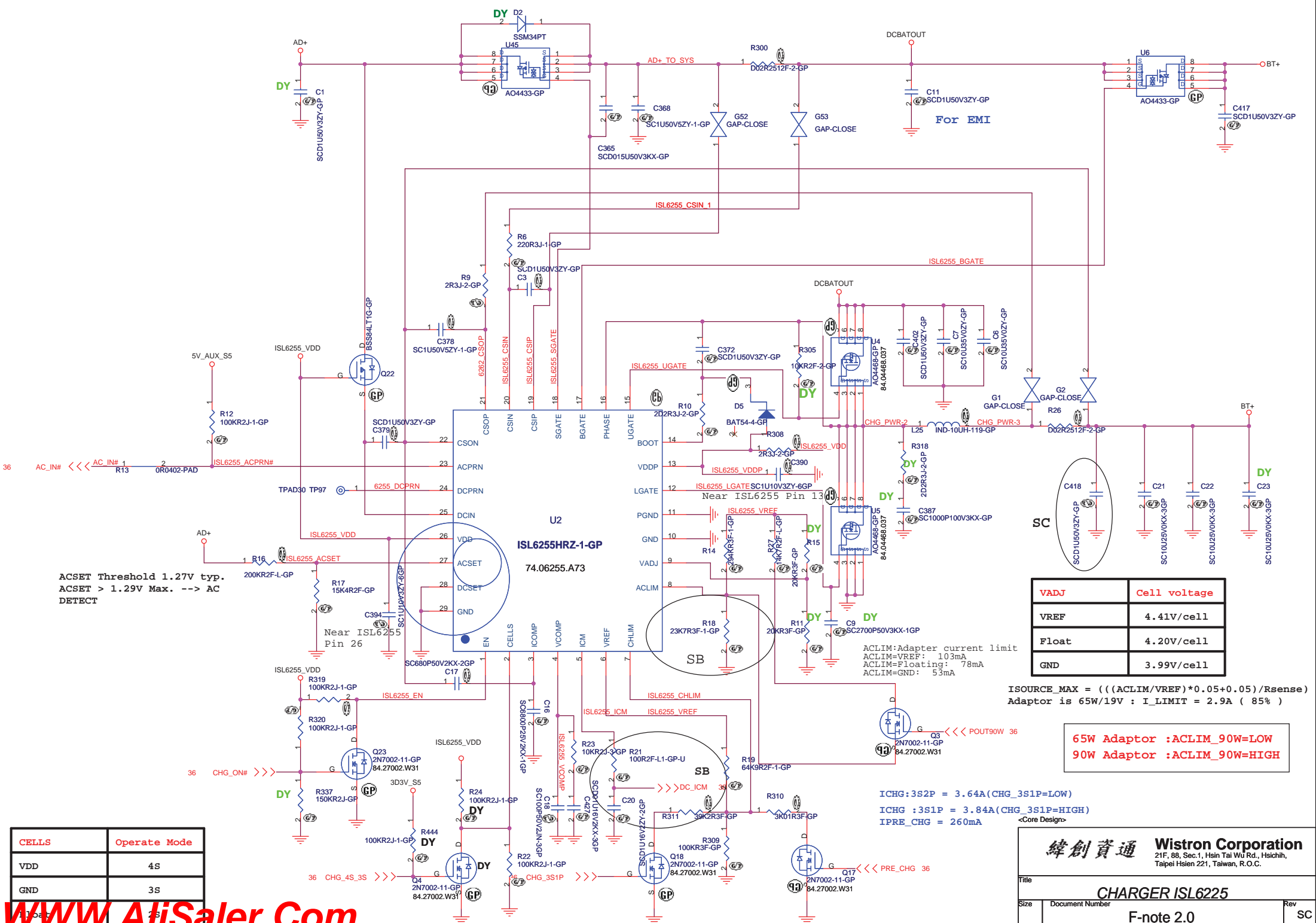
# 1D5V\_SB\_S0 Iomax=3.0A



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Title			LDO 0D9V / 1D25V_S0 / 1D5V_S0
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CELLs	Operate Mode
VDD	4S
GND	3S

VADJ	Cell voltage
VREF	4.41V/cell
Float	4.20V/cell
GND	3.99V/cell

ISOURCE\_MAX = (((ACLIM/VREF)\*0.05+0.05)/Rsense)  
 Adaptor is 65W/19V : I\_LIMIT = 2.9A ( 85% )

65W Adaptor :ACLIM\_90W=LOW  
 90W Adaptor :ACLIM\_90W=HIGH

ICHG:3S2P = 3.64A(CHG\_3S1P=LOW)  
 ICHG :3S1P = 3.84A(CHG\_3S1P=HIGH)  
 IPRE\_CHG = 260mA

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CHARGER ISL6225

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Title

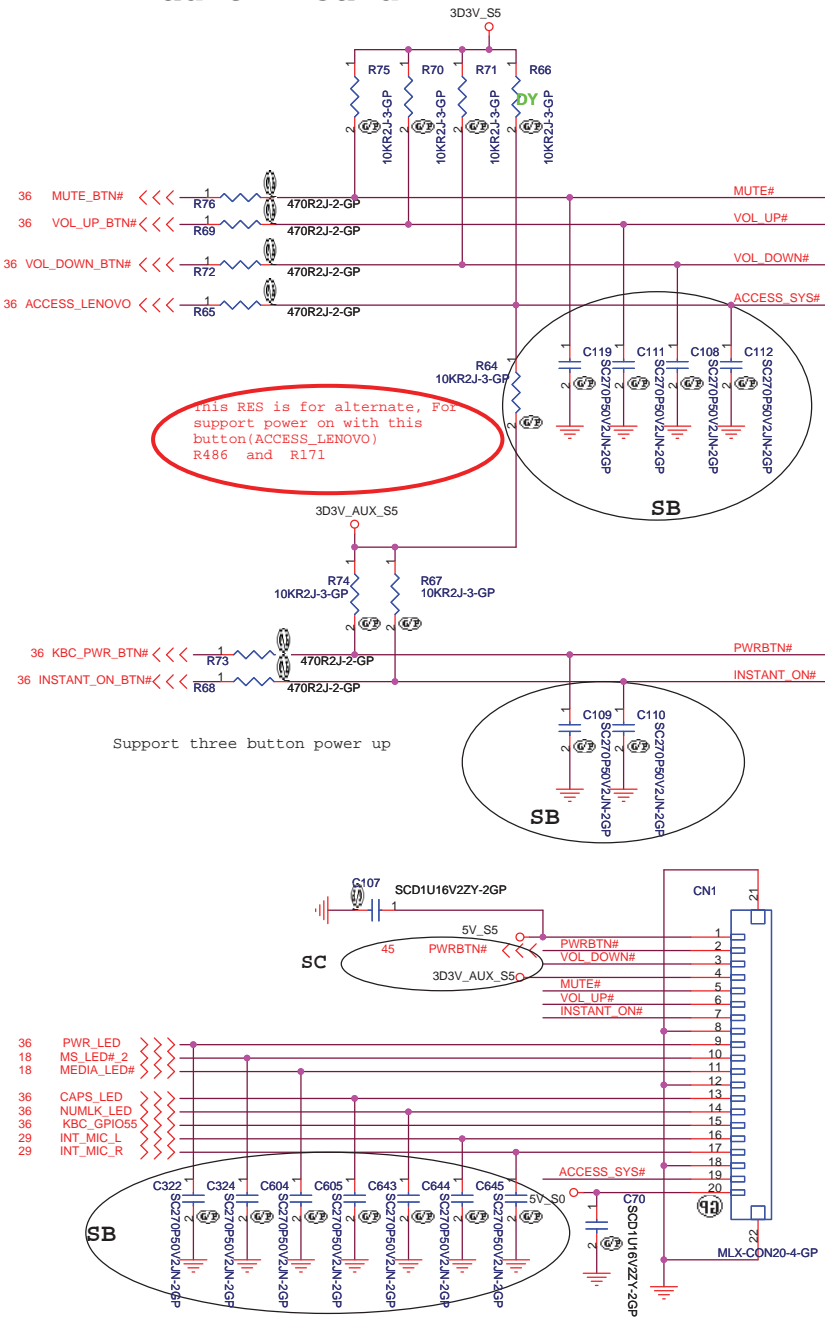
Size

Date: Friday, March 09, 2007

Document Number

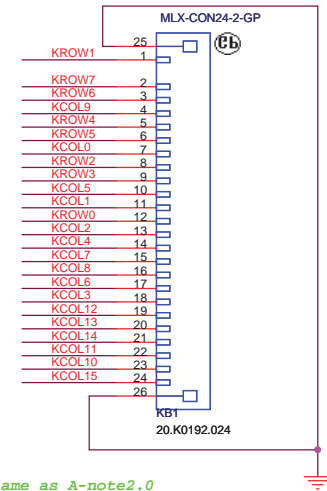
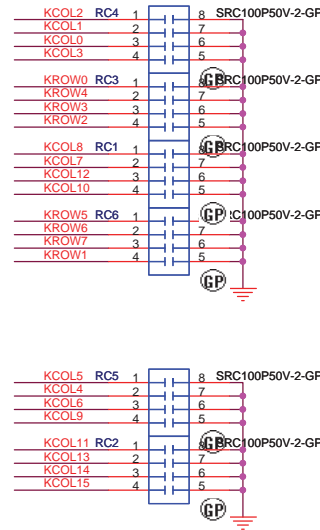
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# Launch Board



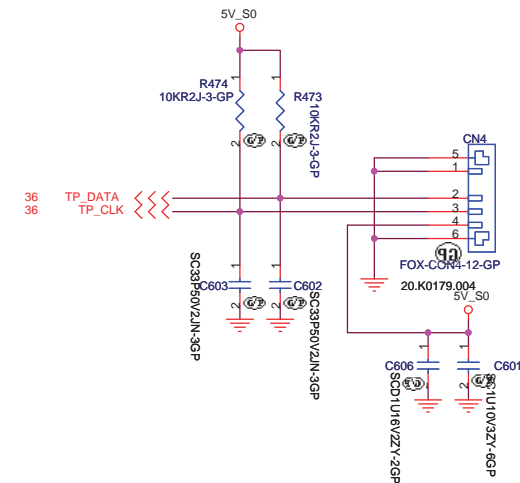
36 KROW[0..7] <<<  
36 KCOL[0..15] <<<

## KeyBoard



The pin define same as A-note2.0

## TouchPad Connector

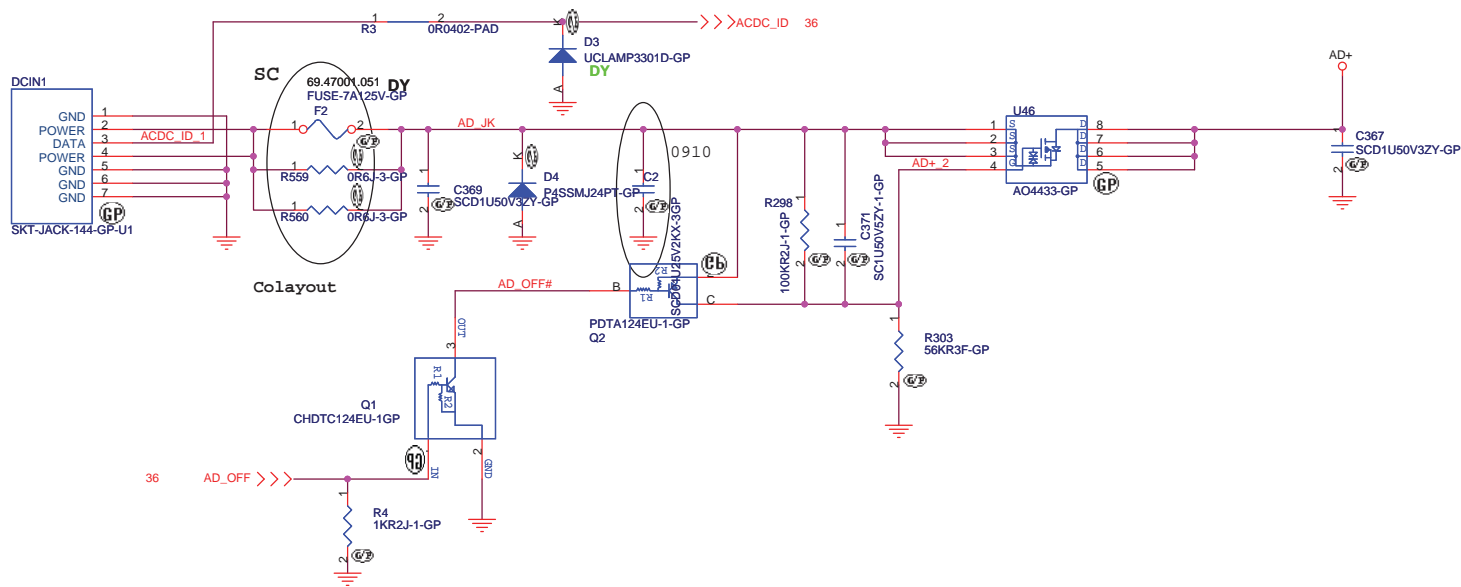


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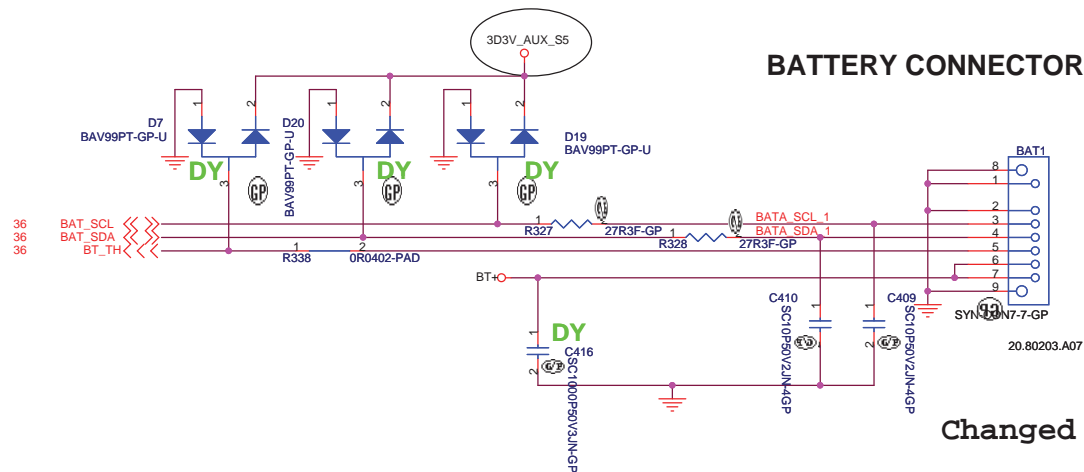
緯創資通 Wistron Corporation  
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Title		KeyBoard&TouchPad&Launch B/D	
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## Adaptor in to generate DCBATOUT



## BATTERY CONNECTOR



Changed

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Title
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### Clock generator CY28548

Size

Document Number

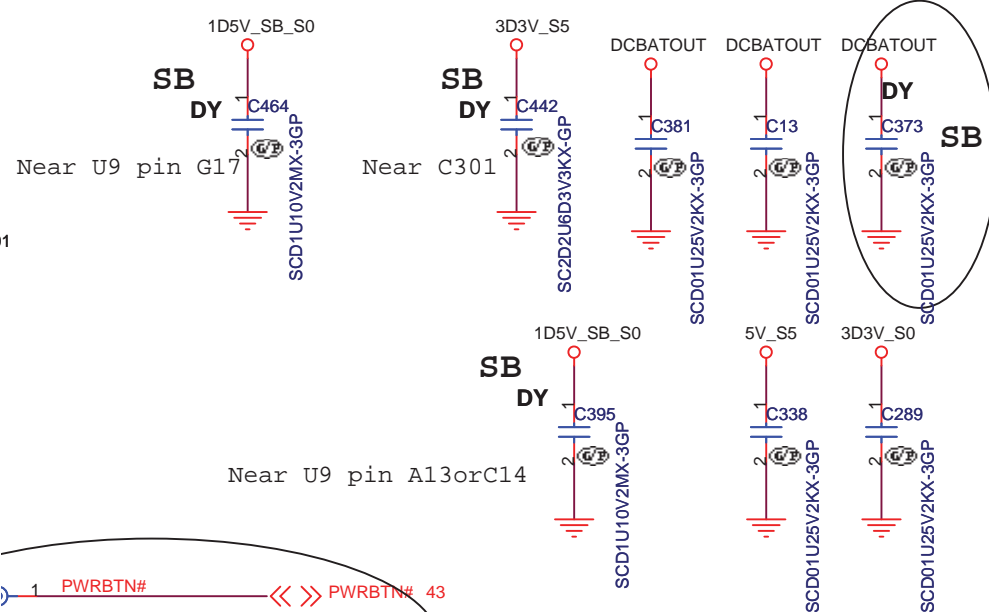
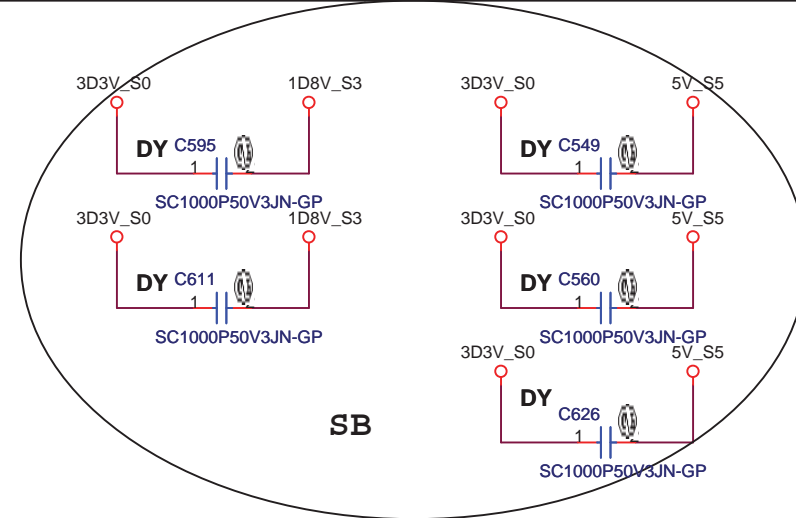
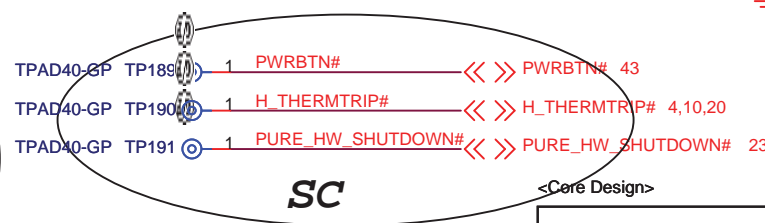
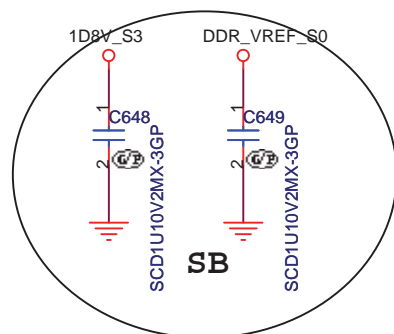
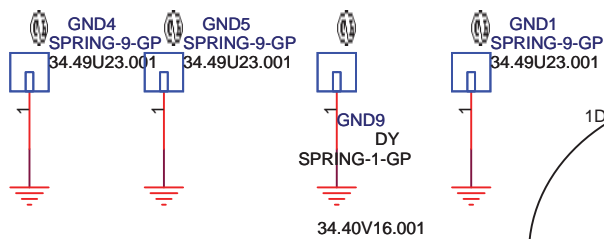
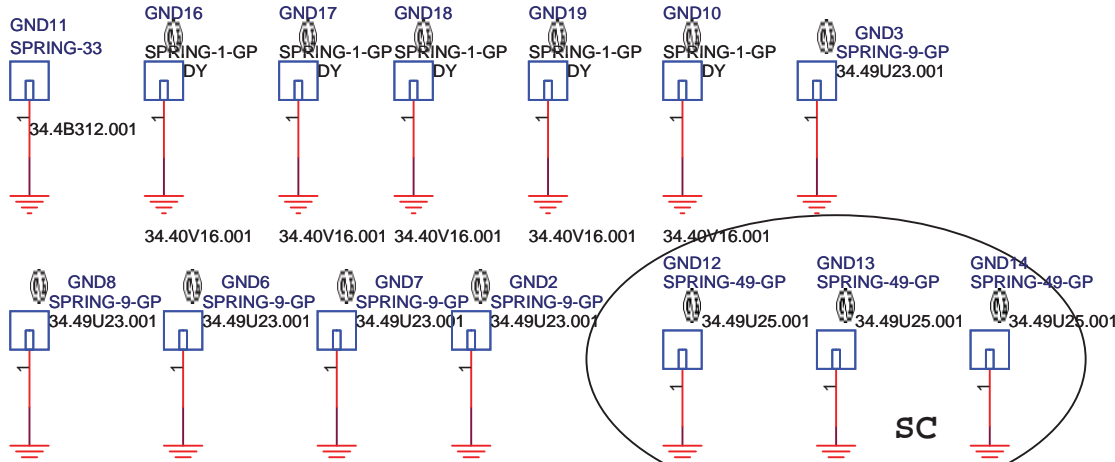
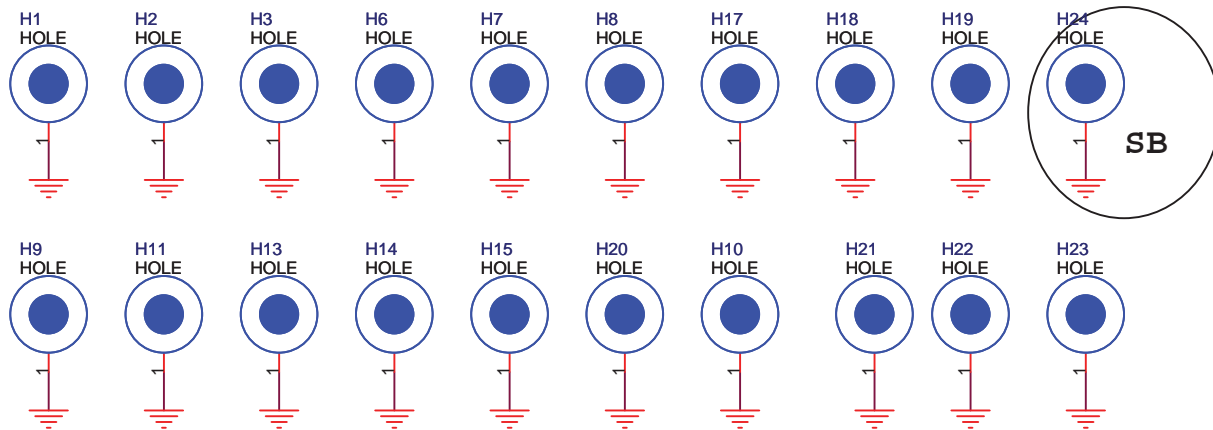
## F-note 2.0

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Bypass Capacitors

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Title		
<b>Thermal/Fan Controller G792</b>		
Size A4	Document Number	Rev <b>SC</b>
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